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FOR THE PERIOD
APRIL 1, 1989 THROUGH MARCH 31, 1990
FOR
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UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

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This is the first annual progress report of the research conducted at the Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, under the sponsorship of the Joint Services Electronics Program from 1 April 1989 through 31 March 1990. The research areas include (1) Physical Electronics, (2) VLSI Circuits and Computer Systems, (3) Electronic Systems, and (4) Management Initiatives (discretionary Director's unit). This report summarizes the areas of research, identifies the most significant results, and lists the publications sponsored by JSEP as well as other sponsoring agencies.

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William Kenneth Jenkins
JSEP Principal Investigator
Coordinated Science Laboratory

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SUPPLEMENTARY UNIT (Partially supported by JSEP)

EXECUTIVE SUMMARY

I. Summary of the Program

The current JSEP program that began on October 1, 1989, retains many features of the elements of the previous program, although there have been considerable changes in the format of the overall program, many changes within the new units, and numerous changes in personnel. There has been a serious effort to reduce the total number of JSEP units in order to consolidate the funding more effectively and to assure that a critical level of support is provided to each project. This has resulted in a reduction to 18 new regular units from our previous number of 22 units. There has also been an effort to involve new faculty where possible, especially in cases where their technical expertise adds new strengths to the JSEP program. Please note that this annual report, which covers the period April 1, 1989 through March 31, 1990, includes research that was supported during the final 6 months of the previous JSEP contract (April 1, 1989 - September 30, 1989) as well as the first 6 months of the new JSEP grant (October 1, 1989 through March 30, 1990). This report is organized around the structure of the new grant and emphasis is placed on the research projects that are supported in the current program. Many of these projects continue along the lines of their predecessors in the previous JSEP contract, while others are new projects that only began on October 1, 1989.

In August 1986 former CSL Director and JSEP Principal Investigator T. N. Trick became the Head of the Electrical and Computer Engineering Department. From August 1986 through May 1987, Professor W. K. Jenkins served as the Acting Director of CSL. From May 1987 until the present, he has been serving as the Director of CSL and as Principal Investigator on the JSEP contract. During the summer of 1987 Professor Jenkins appointed a JSEP Internal Advisory Committee to provide a management structure to the CSL JSEP program. Professor Karl Hess was appointed as the Technical Advisor for physical electronics, Professor Michael Pursley for electronic systems, and Professor Timothy Trick for VLSI circuits and devices. Professor Trick's participation also provides coordination with the Electrical and Computer Engineering Department and the faculty in the new

Microelectronics Laboratory, which is helpful to faculty who participate in the JSEP program but who are not full-time residents of CSL. Professor Hess's participation provides a similar coordination with research activity in the n^wly established Beckman Institute. The JSEP Internal Advisory Committee played a vital role in the formulation of the current JSEP program, and it will continue to advise the Director throughout the 3-year grant period.

The new JSEP program consists of 18 units that are organized into four major areas; three are technical areas and one is managerial. The four areas are: (1) Physical Electronics, (2) VLSI Circuits and Computer Systems, (3) Electronic Systems, and (4) Management Initiatives. Each unit is described briefly below and is explained more completely in the body of this report.

Physical Electronics

Unit 1 is a project by Professor J. Greene on low-energy ion/surface interactions during metal and semiconductor crystal growth from the vapor phase. This work is a continuation of Professor Greene's work on the previous JSEP contract, with the overall scope and personnel continuing at the same level.

In Unit 2 Professors K. Hess and U. Ravaioli are continuing to expand the science of computational electronics for semiconductor devices. They are engaged in a new effort to merge Monte Carlo methods and hydrodynamic models to provide a higher degree of sophistication to device simulation. Assistant Professor Ravaioli joined Professor Hess's group two years ago and is now supported on the JSEP program due to his outstanding contributions in computational electronics.

Professor K. Cheng has joined Professor G. Stillman on Unit 3 in researching new studies for gas source MBE/CBE for optoelectronic devices. Professor Cheng was a Visiting Associate Professor during the 1987-88 academic year, and he has been a regular Associate Professor since fall 1988. He brings to the project a great deal of experience and expertise in MBE/CBE technology.

Professor J. Coleman (Unit 4) has undertaken new work in heterostructure electronic devices by MOCVD technology, which is a continuation of his previous JSEP-supported research. He up-graded his MOCVD system when he moved into the new Microelectronics Laboratory during the summer of 1989. During year one, a portion of the JSEP Director's Fund was used to help fund some of Professor Coleman's new MOCVD equipment (see Unit 18).

In Unit 5, Professors J. Lyding and J. Tucker are using Lyding's recently developed scanning tunneling microscope for the characterization of semiconductor heterolayers and devices. The superb imaging capability of the newly developed scanning tunneling microscope allows experimental investigations of heterolayers that were not previously possible.

In Unit 6, Associate Professor M. Kushner has joined Professors G. Eden and J. Verdeyen in a major new effort to develop a reproducible semiconductor frequency standard with devices based on rare earth ions incorporated into III-V materials. This work represents a major change in direction for Professors Eden and Verdeyen from their previous JSEP project on the chemistry of excited state gases. It was possible to accommodate M. Kushner in this project with funds that were released by the late J. Thornton's unit at the end of the previous JSEP contract. Professor Kushner assumed responsibility for Thornton's unit at the time of his death in November 1987, bringing that work to a successful termination by September 30, 1989.

Unit 7 is a direct continuation of work that was started as a new unit in the second year of the previous JSEP contract by Professors I. Adesida, J. Kolodzey, and J. Leburton. This unit addresses the problems of electronic and transport properties of ultra-low-dimensional semiconductor structures. This new research represents a team approach, with J. Leburton providing important theoretical expertise, I. Adesida providing experimental expertise, and J. Kolodzey providing key skills in high-speed device measurements. This unit has already made important advances in the conception and verification of a new tunneling mechanism in MODFET structures and, as such, was cited as one of the most significant accomplishments of the previous JSEP contract.

Unit 8 also represents a major change in direction for Professor R. Mittra from his previous JSEP-supported work in electromagnetic scattering. In this unit he is working with Assistant Professor J. Schutt-Aine in a project on electromagnetic modeling and simulation of high-speed digital circuit interconnections. They are applying their expertise in electromagnetics to develop a better understanding of the behavior and performance of interconnections in microelectronic packaging and high-speed digital network applications. Note that although this work is essentially in electromagnetics, it has been grouped with the Physical Electronics area to emphasize its importance in high-speed devices. *VLSI Circuits and Computer Systems*

Units 9 and 10 support the work of Professors Patel, Hwu, Banerjee, Fuchs, and Iyer of the Computer Systems Group at CSL. Unit 9 addresses important problems in high-performance computer architectures, with J. Patel and W.-M. Hwu as the primary participants. Their objective is to develop, model, and analyze efficient, high-performance computer architectures that will exploit both high-density and high-speed semiconductor technologies. Assistant Professor Hwu joined the faculty in the fall of 1987 as a graduate of Berkeley and is now participating in the JSEP program for the first time. Professors Banerjee, Fuchs, and Iyer conduct the research of Unit 10 on VLSI circuits and computer systems. This unit explores concepts in reliable computing that will provide an understanding of the basic principles in design and analysis of reliable VLSI-based parallel computer architectures.

The senior investigators on Unit 11 are Professors F. Preparata, M. Loui, and B. Wah. The emphasis in Unit 11 is on the analysis and design of efficient computation techniques, with the dominant theme being parallel computation that leads to suitable structures in VLSI. Note that emphasis in this unit is on the development, analysis, and design of efficient structures (algorithms), whereas the emphasis in Units 9 and 10 is on machine design and machine architecture.

The research on Unit 12 is conducted by Professors I. Hajj, S. Kang, and V. Rao on the subject of computer-aided design of very high-speed integrated circuits. The objective of their work is to develop analysis and design techniques for reliable high-speed integrated circuit designs. This includes the automatic synthesis of testable circuits with a reduced number of devices, automatic generation of layout using two metal interconnects, and the development of mathematical methods and algorithms for optimizing the design.

Electronic Systems

Units 13 and 14 are research projects in the control systems area. Professors Kokotovic, Kumar, and Poolla are conducting the research on Unit 13, which seeks to develop a fundamental understanding of how to design high-performance and robust adaptive systems for use in control, filtering, estimation, and identification. In particular, they are studying some important issues concerning the fundamental behavior of least squares parameter estimators, such as stability and convergence, and they will also investigate the self-tuning properties and robustness of adaptive systems. The research of Unit 14 is conducted by Professors T. Basar, J. Medanic, and W. Perkins on the topic of decentralized and distributed control of large dynamic systems. This work has applications to aircraft control, ship steering, vibration control of large flexible space structures, and remote control and navigation of all-terrain vehicles.

Professors Y. Bresler, T. Huang, and D. Munson are the senior investigators on Unit 15, which is a study of sensor-array imaging techniques for dynamic scenes. This work in signal processing has important applications in synthetic aperture radar (SAR), X-ray computer tomography (CT), and scanning laser range finders, to name a few. The objective is to study basic issues in using sensor arrays to image dynamic scenes, particularly ones in which the amount of object motion or scene change is significant during the time interval used to collect each image frame. Note that Assistant Professor Y. Bresler is new to the JSEP program, having joined the faculty in the fall of 1987 after serving as a post-doctoral research associate at Stanford following his graduation from there in 1986.

In Unit 16 Professors B. Hajek, M. Pursley, and D. Sarwate are researching topics in survivable communication networks. Their objective is to improve the state of the art by investigating critical issues in communication network design and performance. In particular, they seek a better understanding of the fundamental trade-offs between communication efficiency and survivability. They are working with improved modulation and coding schemes, receiver processing techniques, and network protocols for use in communication networks that are likely to be subjected to jamming, fading, and loss of resources.

Unit 17 is a new research effort by Professors K. Arun, K. Jenkins, D. Jones, and V. Poor on adaptive signal processing, which seeks to develop new methods to extract and/or enhance time-varying (nonstationary) signals from additive noise. Both parametric and nonparametric approaches will be investigated in this project for both narrow-band and wide-band signals of interest. The overall objectives are to develop computationally efficient adaptive time-frequency representations and new adaptation algorithms and filter structures that are computationally efficient for real-time applications, are robust, and are suitable for short wordlength VLSI implementation. Assistant Professor D. Jones joined the faculty in fall of 1988, after spending a year as a Fulbright post-doctoral fellow at the University of Erlangen-Nuremburg following his graduation from Rice University.

Management Initiatives

Unit 18 provides the Director with discretionary funds to support early start-up on new projects that present immediate opportunities of high scientific promise, to provide matching funds for new equipment, and to support promising work of new faculty whose interests are closely aligned with the JSEP program, but who are not presently supported. During the first year of the current JSEP grant, four specific projects have received support from JSEP discretionary funds. These include support toward an upgrade of MOCVD equipment that is housed in the new Microelectronics Laboratory, partial support for a JSEP supplementary project that could not be funded in the regular program (Professor C. Chuang, Unit 20), continuing support of the EpiCenter operating fund, and summer support for several new faculty who are contributing to the current JSEP program. Details of these projects are reported in the main body of this first-year JSEP report under Unit 18.

II. JSEP Significant Accomplishments (April 1, 1989 - March 31, 1990)

Two categories of "most significant accomplishments" are reported in this section and cited as important contributions that have been supported either in total or in part by the JSEP grant at the University of Illinois at Urbana-Champaign. In the first category, we cite three outstanding technical accomplishments that were direct results of JSEP research. Further details on these accomplishments are discussed in the main body of this report. In the second category, we cite the accomplishments of three individuals who have received JSEP support over the years through the Coordinated Science Laboratory and who have been indirectly nurtured in their accomplishment by JSEP support.

A. Recent Outstanding Technical Results

i) A New Technique for Tomographic Imaging of Time-Varying Distributions (Unit 15)

A novel technique for tomographic imaging of time-varying distributions has been developed by Professor Y. Bresler and his research assistant, N. P. Willis [1]. This technique is applicable when the temporal variation during acquisition of the data is high, precluding Nyquist rate sampling, and a-periodic, precluding reduction to the time-invariant case by synchronous acquisition. The technique involves an unconventional order of sampling the projections, which is designed to minimize the energy of the reconstruction error of a representative test image. In computer simulations, a 7-fold decrease in the error energy was observed using the optimized sampling scheme, compared to conventional sampling. The results indicate the potential for efficient acquisition and tomographic reconstruction of time-varying data. Application of these techniques is foreseen in SAR imaging, X-ray computer tomography, and magnetic resonance imaging. An invention disclosure on the technique was filed with the University of Illinois and is currently under evaluation for possible patent application [2].

ii) A New Error-Control Algorithm that "Beats" the Computational Cut-Off Rate (Unit 16)

Professors Arikan* and Hajek and their research assistant B. Radosavljevic invented and investigated a new method of providing forward error correction, based on a new procedure for decoding certain block codes [3]. The new decoding algorithms, called sequential decoding with reordering (SDR) algorithms, observe the received message at a communication channel output and use this information to reorder the digits in the codeword tree. The resulting tree is then searched by a sequential decoder; the goal of the reordering is to obtain a tree that is easy to search. Linear block

*Professor Erdal Arikan was with the University of Illinois and was supported by the JSEP Program. He is now with the Department of Electrical and Computer Engineering at Bilkent University, Ankara, Turkey.

codes are used in which each parity check involves a small number of bits (low-density parity check codes).

Simulations completed this spring demonstrate that the new decoding method allows computationally feasible operation at data rates above the well-known computational cut-off rate for channels with low erasure or error probabilities. This is significant since, at such high data rates, the mean computation required per data bit is infinite for any traditional sequential decoding procedure. The new method can thus potentially increase the rate of reliable communication over noisy communication channels with computationally feasible decoding algorithms at the receiver.

iii) Design and Implementation of High-Performance Fault Recovery in Hypercube Multiprocessors (Unit 10)

In the past year, Professors Banerjee and Fuchs and their research assistants M. Peercy and C. C. Li have derived important new results concerning hardware and software approaches to high-performance recovery from faults in parallel hypercube-based multicomputer systems [4,5]. The results include flexible schemes for reconfiguration around faulty processor nodes, techniques for optimal rerouting in the presence of faults, and a method for process checkpointing and rollback recovery in hypercube parallel architectures. Their reconfiguration results include four schemes for reconfiguration, two in hardware that use spare processor nodes and interconnections and two in software that require no hardware modification. The schemes for reconfiguration and message rerouting have been implemented on an Intel iPSC/2 hypercube and have been demonstrated to provide high-performance fault recovery. These new techniques for process checkpointing and recovery have been shown to provide effective on-line tolerance of hypercube failure.

B. Outstanding Professional Accomplishments of JSEP-Supported Faculty

i) Professor Gregory E. Stillman, University of Illinois at Urbana-Champaign

Professor G. Stillman and Dr. Charles M. Wolfe, Washington University, St. Louis, MO, were jointly named as the 1990 winners of the IEEE Jack A. Morton Award "for the growth and characterization of ultrahigh purity gallium arsenide and related compounds." Stillman developed a new far-infrared spectroscopic technique, Fourier transform photothermal ionization spectroscopy, which detects and identifies shallow donor species at concentrations in the part-per-billion range or below. Along with Wolfe, Stillman applied this technique to the characterization of ultrahigh-purity epitaxial gallium arsenide. Both men were then at the Massachusetts Institute of Technology's Lincoln Laboratory. The ability to produce ultrahigh-purity gallium arsenide led to a number of unforeseen applications, including extrinsic far-infrared photoconductors, avalanche photodiodes, and electron-beam-semiconductor devices [6].

ii) Professor Miles V. Klein, University of Illinois at Urbana-Champaign

Professor M. Klein was named the 1990 winner of the Frank Isakson Prize for Optical Effects in Solids "for his pioneering experimental and theoretical contributions to many aspects of our understanding of light scattering in solids, particularly Raman scattering from impurity modes in insulators, folded phonons in semiconductor superlattices, and from electronic excitations in superconductors." The Prize address was delivered at the March 1990 Meeting of The American Physical Society in Anaheim, California. The prize was established in 1979 and sponsored by the Photoconductivity Conference. The purpose of the prize is to recognize and encourage outstanding contributions to the field of optical effects in solids.

Professor Klein was supported by the JSEP contract for many years until his appointment as Director of the Illinois Superconductivity Center required him to withdraw his participation in 1987. In particular, Professor Klein worked with a post-doctoral fellow, Dr. Roberto Merlin, on the topic of folded phonons under JSEP-sponsored research in the 1979-1980 time frame.

iii) Dr. William Rouse, Search Technology, Inc.

The March 1990 issue of *Spectrum* magazine featured an article entitled "Computer-Aided Fighter Pilots," co-authored by W. Rouse, N. Geddes, and J. Hammer, of Search Technology, Inc. [7]. Dr. Rouse began his career at CSL with support from the JSEP program. He later joined the faculty at Georgia Institute of Technology and then went on from there to become the founder of Search Technology, Inc. Early JSEP support contributed to the success that Dr. Rouse is experiencing today in doing important work for the Department of Defense, as evidenced by the recent *Spectrum* article that he co-authored.

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WORK UNIT NUMBER 1

TITLE: Low-Energy Ion/Surface Interactions during Metal and Semiconductor Crystal Growth from the Vapor Phase: Control of Microstructure and Microchemistry on the Atomic Scale

SENIOR PRINCIPAL INVESTIGATOR:

J. E. Greene, Research Professor

SCIENTIFIC PERSONNEL AND TITLES:

D. Lubben, Postdoctoral
F. Adibi, Graduate Student
T. Bramblett, Graduate Student
L. Markert, Graduate Student
J.-P. Noël, Graduate Student

SCIENTIFIC OBJECTIVE:

The primary objective of this research program is to develop a detailed understanding of energetic particle/surface interactions for controllably altering nucleation and growth kinetics, microchemistry, and physical properties of metal and semiconductor films during deposition from the vapor phase by a variety of techniques including ion-assisted MBE, plasma-assisted CVD, sputter deposition, and primary-ion deposition. Low-energy ion/surface interactions allow the crystal grower additional dynamic control, at the atomic level, over microchemistry and microstructural evolution. Kinetic energy can be efficiently coupled to the growth surface thereby altering surface reactivity as well as adsorption, adatom diffusion, and nucleation kinetics. The ability to use such effects to advantage in "designing" new growth processes as well as new materials depends upon our understanding of the nature of ion/surface interactions, as well as thermal adatom/surface reactions, during deposition. This work is being pursued from both an analytical and an experimental point of view.

SUMMARY OF RESEARCH:

Surface Reactions, Elemental Incorporation Mechanisms, and Depth Distributions of Thermal and Accelerated Dopants During Si MBE

As device sizes continue to shrink, not only laterally, but in depth, control of microchemistry at the atomic level becomes ever more important. One area in which this has immediate consequences is dopant incorporation in semiconductor films grown from the vapor phase. Incorporation may be limited not just by the initial sticking probability (i.e., the probability of chemisorption) but also by the combination of surface segregation and desorption. Surface segregation, in addition, results in dopant profile broadening These problems are particularly acute in MBE Si where most of the common dopants used in bulk Si technology present problems when co-evaporated during film growth due to low incorporation probabilities (P, As, Sb, Ga, and In) and/or pronounced surface segregation (As, Sb, Al, Ga, and In).

As reported previously, we have developed a general time-dependent model, which combines thermodynamic and kinetic elements, for describing the incorporation of dopants during vapor-phase deposition. The model accounts for dopant segregation and allows elemental incorporation probabilities σ and depth-dependent concentration profiles C(x,t) to be calculated as a function of experimental parameters such as film and dopant material, deposition rate R, incident dopant flux J, growth temperature T_s, etc. Calculated profiles from arbitrarily complex doping schedules are in excellent agreement with available experimental data for both acceptor and donor dopants in MBE Si. "Anomalies" in previously published data have now been explained, using the model, as being due to variations in desorption and/or (depending upon the dopant) surface-segregation kinetics that occur in response to changes in T_s and dopant surface coverage θ. In addition, we have used the model to predict new phenomena such as critical temperatures in dopant segregation regimes, dopant-induced surface structural phase transitions, and changes in dopant/surface reaction paths leading to modifications in surface binding energies and hence dopant incorporation probabilities. All of these phenomena have now been observed experimentally.

We have recently predicted that there should exist a narrow growth temperature window over which abrupt doping profiles can be obtained for Al, an important p-type dopant that exhibits severe surface segregation during MBE Si and has generally been acknowledged in the literature to be unusable in MBE Si. We have confirmed the predictions experimentally and demonstrated, for the first time, relatively abrupt modulation-doped Al profiles. σ_{Al} was found to vary from $\simeq 0.2$ at $T_s = 525$ °C to 9×10^{-5} at 975 °C with R = 1 μm h^{-1} and $J_{Al} = 3\times10^{11}$–1.5×10^{12} cm^{-2} s^{-1}. Extreme profile broadening Δ_{Al} due to dopant surface accumulation was observed at low growth temperatures with $\Delta_{Al} \simeq 600$ nm/concentration-decade at $T_s = 775$ °C. In fact, at $T_s \leq 825$ °C, θ_{Al} was large enough (> 0.2 ML) to give rise to the formation of an Al-stabilized (1x1) RHEED pattern. At higher growth temperatures, the Si(100)2x1 pattern was restored. There was a narrow range near 875 °C over which the Al desorption rate was sufficiently high and bulk diffusion rates sufficiently low to allow the formation of relatively abrupt doping profiles with interface widths more than an order of magnitude lower than those obtained at lower temperatures. At higher growth temperatures Δ_{Al} increased again due to bulk diffusion. Hall effect measurements showed complete electrical activity with mobilities comparable to those of B-doped bulk Si.

Our general approach for resolving the problems of low dopant incorporation probabilities and high segregation rates during Si MBE has been to employ accelerated-beam doping techniques using unique UHV-compatible, low-energy, high-brightness, ion sources developed under JSEP sponsorship. During this past year, we have extended our work on In^+ ion doping (where we demonstrated increases in σ_{In} by more than 6 orders of magnitude and the first example of δ–doping during MBE Si) to Sb^+. The kinetics of dopant incorporation were determined experimentally as a function of acceleration potential E_{Sb} = 0-200 V, T_s = 550-1050 °C, and R = 0.2-3 μm h^{-1}. σ_{Sb} was up to 5 orders of magnitude higher than attainable using thermal beams. In fact, σ_{Sb} was unity for $E_{Sb} \geq 150$V at $T_s \leq 850$ °C. At lower acceleration potentials, σ_{Sb} was dependent upon T_s and R (following behavior in agreement with the model described below). However, even at $E_{Sb} = 25$ V and $T_s \geq 650$ °C, σ_{Sb} was still more than an order of magnitude larger than for thermal doping. Moreover, surface-segregation-induced profile broadening Δ_{Sb}, which for thermal-beam doping was ≥ 80 nm/decade for $T_s \leq 650$ °C, was less than the SIMS depth resolution, $\simeq 12$ nm/decade.

The results for σ_{In} and σ_{Sb} as a function of E and T_s, at least for E < 200 eV, cannot be described simply as implantation since the projected ion range is of the order of lattice constants. Thus, we have extended our thermal-dopant incorporation model and have developed a multisite transition-state model that explicitly accounts for surface reconstruction and dopant kinetic energy. For example, in the case of MBE growth on Si(100)2x1, the model includes bond rotation and changes in backbond lengths (hence potential barriers) in the first 5 layers (surface, bulk, and three intermediate sites). Surface segregation, dopant desorption, incorporation, and bulk diffusion are included and dopant depth distributions are obtained by solving simultaneous transition-rate equations for passage between adjacent sites. Site desorption and segregation potentials were obtained from our previous modulated beam mass spectrometry and thermally stimulated desorption experiments. Model calculations were in extremely good agreement with our experimental data for $\sigma(E_{Sb},T_s,R)$. We are presently combining the analytical results with molecular dynamics simulations discussed below.

Electronic and Optical Properties of Accelerated-Ion Doped MBE Si

An essential question to be addressed in view of the excellent incorporation results obtained for accelerated-beam doping is whether low-energy ion bombardment results in residual lattice damage, which degrades electrical and optical properties. Obviously, at sufficiently high acceleration energies and low growth temperatures this will be the case. In our initial experiments reported last year, we showed that for Si films grown at $T_s = 800$ °C, $E_{In} = 200$ eV or $E_{Sb} = 150$ eV, and R = 1-2 μm h^{-1}, all dopant atoms were incorporated into electronically active substitutional sites at concentrations at least up to $2x10^{18}$ cm^{-3} for In (exceeding the solid-solubility limit) and $2x10^{19}$ cm^{-3} for Sb. Temperature-dependent Hall measurements showed that carrier mobilities were equal to calculated theoretical limits (in fact, the In^+ doped films exhibited the highest mobilities ever reported for In-doped Si, film or bulk!).

We have recently begun to apply more stringent probes: temperature-dependent photoluminescence (PL) and deep-level transient spectroscopy (DLTS). In the initial experiments, we have grown a series of 5-μ m-thick As^+-doped films with concentrations between $2x10^{16}$ and $5x10^{17}$ cm^{-3} using E_{As} = 200-1000 eV at T_s = 500-800 °C. σ_{As} was essentially unity in all cases (for thermal doping σ_{As} is unmeasurable, < 10^{-8}). The ion-doped films exhibited the first high-quality PL spectra ever reported for doped MBE Si. Sharp ($\leq$ 0.5 meV FWHM), very intense, no-phonon and TO and TA phonon-assisted bound exciton peaks were obtained. No peaks ascribable to residual ion-induced damage were observed in films grown at T_s = 800 °C with $E_{As} = \leq 1000$ eV or $T_s = 650$ °C with $E_{As} = 200$ eV. In fact, these films exhibited two-phonon (TO + Γ) assisted bound exciton peaks, indicative of very high quality material. DLTS measurements have shown no indication of deep traps in any of these films to within the resolution of the measurement (1012 cm-3).

However, reducing T_s to 500 °C with E_{As} = 200 eV gave rise to a strong ion damage PL peak at 1039.7 meV. Furthermore, both undoped and As^+ doped films grown at 500 °C exhibited a gradual increase in PL background below 890 meV, which we believe was due to quenched-in growth-related point defects. DLTS measurements showed electron trap states ($\simeq 10^{14}$ cm^{-3}) at energies of 0.06 and 0.52 eV below the conduction band edge. Clearly, at growth temperatures near and below 500 °C, E_{As} will have to be decreased below 200 eV and we have now grown some samples with E_{As} = 50 eV. In addition, the PL results for undoped films indicate that there is a substantial number of growth-related defects which are not annealed out during deposition at $T_s = 500$ °C.

Molecular Dynamic Simulations of Low-Energy Ion/Surface Interactions during Si MBE: Accelerated-Ion Doping and Low-Temperature Epitaxy

We have developed a supercomputer code for carrying out molecular dynamics (MD) simulations, utilizing the Tersoff many-body potential, to investigate ion/surface interaction effects. The MD simulations are presently being used in conjunction with our analytical model of ion doping described above to understand the details of collisional lattice dynamics and ion-induced defect formation and annihilation. In addition, the simulations are providing, for the first time, insights into potential mechanisms for ion-irradiation-induced "low-temperature" epitaxy, which has been reported by a number of groups for systems such as Ag/Si, Si/Si, and InAs/Si.

Our initial simulations were carried out for 10 eV Si atom bombardment of a Si lattice with a (001)2x1 reconstructed surface. The irradiation events were initiated at an array of points in the primitive surface unit cell. Each event was followed to determine kinetic energy redistribution in the lattice as a function of time, ion and lattice atom trajectories, and the nature, number, and depth of residual defects. Surface dimer breaking, epitaxial growth (due to both projectiles and lattice atoms coming to rest at epitaxial positions), and the formation of residual hexagonal and split interstitials composed of projectiles and/or lattice-atoms were observed. There were no residual vacancies. Impact points leading to each of the above results clustered in distinctly different regions of the surface unit cell. Quasidynamic simulations showed that the interstitials formed could be annealed out dynamically during film growth at 600 °C in times less than that corresponding to the growth of 1 ML at R = 1μm h^{-1}.

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WORK UNIT NUMBER 2

TITLE: A Merger of Monte Carlo Methods and Hydrodynamic Models in Computational Electronics

SENIOR INVESTIGATORS:

K. Hess, Research Professor
U. Ravaioli, Research Assistant Professor

SCIENTIFIC PERSONNEL AND TITLES:

J. Higman, Visiting Assistant Professor
J. Bude, Research Assistant

SCIENTIFIC OBJECTIVE:

The development of physically accurate and computationally efficient device models continues to be of vital interest for the design and analysis of modern silicon VLSI circuits. We have developed in the past very accurate Monte Carlo simulation tools. While these tools cover much of the important physics of fine line devices, they are computationally very intensive. We propose therefore to merge the Monte Carlo methods with more standard approaches in two distinct ways. We believe that in this way we can achieve both physical accuracy and computational efficiency.

SUMMARY OF RESEARCH:

I. Augmented Drift-Diffusion Solver

We have implemented a robust program for the steady-state solution of semiconductor device equations based on an augmented drift-diffusion approach. Drift-diffusion (D-D) models still constitute the backbone of detailed device simulations, particularly in connection to device optimization and circuit simulation. As device dimensions have shrunk to submicron levels, the traditional current equation, which describes only velocity saturation of the hot-electron effect, becomes inadequate because velocity overshoot effects can be very important. An alternative way, the Monte-Carlo (MC) method, offers a rigorous description of semi-classical device physics but still requires very large computational resources and cannot be applied extensively to realistic device structures with high dopings. Thornber [17] has suggested a one-dimensional augmented D-D equation for modeling velocity overshoot effects. A number of simulation experiments in connection to this proposal have been performed for Si [18-20].

To effectively implement the augmented D-D equations proposed by Thornber, as well as other alternative similar approaches, a simulator should be [21]:

(1) simple to modify so that the existing code can accommodate different formulations of the equations with minimal knowledge of the numerical details of the simulator program;

(2) simple to use so that new algorithms, geometries, and models can be tested efficiently;

(3) numerically rigorous and stable to guarantee convergence and accuracy; and

(4) consistent with the data transfer standard to link with other simulation tools [22].

With these ideas in mind, we implemented a new D-D device simulator in collaboration with Professor Thomas Kerkhoven of the Computer Science Department. The simulator is called OSMOSIS (OverShoot Modeling Of SemIconductor Structures). The code uses the box integration method over a nonuniform rectangular grid. Based on a more flexible current equation formulation [23], the 1-D steady-state augmented drift-diffusion equation proposed by Thornber has been implemented, using the following mobility and diffusion coefficient [20]:

$$\mu(E) = \mu_{LIS}(E) \cdot (1 + \frac{L(E)}{E}\frac{dE}{dx}) \tag{1}$$

$$D(E) = \frac{k_B T}{q}\mu_{LIS}(E) \tag{2}$$

Here, E is the electric field and $\mu_{LIS}(E)$ includes the lattice and impurity scattering and the velocity saturation effects. The length coefficient $L(E)$ is an input that includes the overshoot information. For Si, $\mu_{LIS}(E)$ is most often modeled using the Caughey-Thomas expression [24].

$$\mu_{LIS}(E) = \frac{\mu_{LI}}{\left[1 + \left(\frac{E}{E_{crit}}\right)^{\beta}\right]^{1/beta}} \tag{4}$$

$$\mu_{LI} = 88\frac{cm^2}{Vs}\cdot\left(\frac{T}{300}\right)^{-0.57} + \frac{1252\frac{cm^2}{Vs}\cdot\left(\frac{T}{300}\right)^{-2.33}}{1 + \frac{CI}{CI_{crit}\cdot\left(\frac{T}{300}\right)^{2.546}}} \tag{5}$$

where CI is the impurity concentrations. We have tested the simulator on an n^+–n–n^+ 1-D Si device and the results in Figure 1 show the difference in the drift velocity obtained at a given bias point, with and without the overshoot terms. By this implementation, we demonstrate the capability and flexibility of our simulator. Other models can be adapted into the simulator with very little effort thanks to the program structure. In addition, although we have tested so far 1-D cases, the code treats a 2-D discretization so more complex devices can be studied, provided that the augmented drift-diffusion model is properly extended to 2-D. Future developments of the simulator include a more user-friendly interface, a standardization of data transfer format, and extension to higher dimensionality. In parallel, a theoretical investigation on the overshoot model is carried on, since the use of just a length coefficient $L(E)$ may not be sufficient for III-V semiconductors.

II. Impact Ionization in Si Photodetectors

We have applied previously developed Monte Carlo models to two different problems in which nonstationary effects due to the inhomogeneity of the field are important. First, we have undertaken an analysis of the impact ionization process in Si photodetectors in collaboration with R. J. McIntyre (G.E. Canada). In this work we investigate theoretically the nonlocality of impact ionization in semiconductors due to the history of the carriers as well as the inhomogeneity of the electric field. We

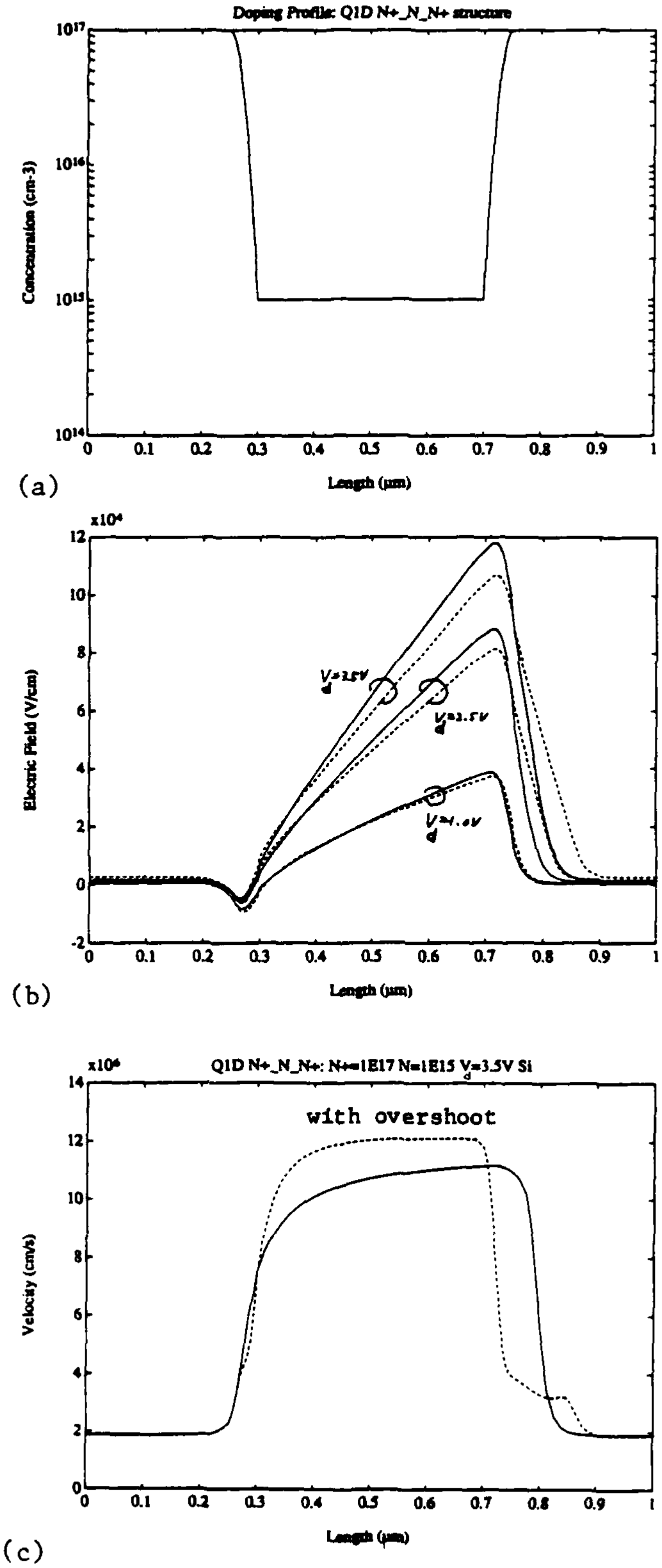

Fig. 1. (a) Doping profile of the simulated structure; (b) Electric field distribution at various bias voltages; (d) Drift velocity for a bias $V_d = 3.5V$. Solid curves refer to results with simple drift-diffusion; broken curves include the overshoot term in the mobility.

point out its significance for the calculation of noise in APD's and calculate the necessary ionization coefficients.

We have investigated in detail the case of electrons in silicon at room temperature, for which the Monte Carlo transport model is believed to be reasonably well understood. The Monte Carlo model was used to compute a function that we have introduced, which will be referred to as the ionization coefficient kernel. This kernel is a function of both the point at which the electron is assumed to have relatively little energy (i.e., the electron was either injected from a low field region or is one of the two electrons resulting from an ionizing collision) and the current position. Such Monte Carlo calculations have been carried out for a variety of one-dimensional electric field profiles.

For the relatively simple case of injection from a low field region into a large uniform field, the ionization kernel is found to remain near zero for a distance over which a potential drop of 2-3 Volts is encountered (dead space) and then rises for a short distance to a value larger than the homogeneous field value. For the more complicated case of linearly varying fields with a slope in the range 10^9–10^{10} V/cm^2, the average ionization coefficient can be different from the local-field-dependent (uniform field) value by an order of magnitude due to the rapid variation of the field.

The ionization coefficient kernel is necessary for the exact calculation of gain and excess noise factor in avalanche photodiodes. These calculations have previously been possible only by making simplifying approximations regarding the ionization probabilities. This function is not a measurable quantity and can be obtained only from an appropriate solution of the Boltzmann equation as has been done here.

III. Hydrodynamic Semiconductor Equations

We have also undertaken an investigation of the fundamental limitations of the "hydrodynamic" semiconductor equations, in collaboration with W. Fichtner (ETH, Zurich) and W. M. Coughran (AT&T Bell Laboratories). The hydrodynamic model, consisting of the first three moments of the Boltzmann Transport Equation, is known to be incomplete in that an approximate closure relation must be invoked in order to make the system of equations soluble. This closure relation (in practice, a modified Wiedemann-Franz relation between the electrical and thermal conductivity serves this purpose) contains the information of all higher order moments that are not solved. Even for the relatively simple case of a one-dimensional (n+ n n+) silicon diode at room temperature, small changes in this approximate closure relation can cause the hydrodynamic model to converge to unphysical results. Using Monte Carlo simulations to obtain accurate solutions for simple test devices, we have examined the closure relation (i.e., we calculate the thermal conductivity directly) and the energy-dependent energy and momentum relaxation times that appear in the hydrodynamic equations.

Since the project was just begun in October 1989, only one paper has been submitted for publication. However, we are working on several manuscripts based on the results described in this report.

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WORK UNIT NUMBER 3

TITLE: Basic Studies of the Optical and Electronic Properties of Defects and Impurities in Compound Semiconductor Epitaxial Layers and Related Superlattices

SENIOR PRINCIPAL INVESTIGATORS:

G. E. Stillman, Research Professor
K. Y. Cheng, Research Associate Professor

SCIENTIFIC PERSONNEL AND TITLES:

I. Szafranek, Research Assistant
D. Sengupta, Research Assistant
E. J. Roan, Research Assistant

SCIENTIFIC OBJECTIVE:

The objective of this research unit is to contribute to our understanding of impurity incorporation mechanisms, sources, and defects and to improve our understanding of the influence of growth conditions on impurities and defects in semiconductor materials that will be important for new multiple-layer compound heterostructure devices. It includes developing new characterization techniques that will extend the range of impurity concentrations over which quantitative analysis is possible. These techniques will lead to better control of high-purity growth and accurate doping levels in epitaxial layers grown by metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), and chemical beam epitaxy (CBE) or gas source molecular beam epitaxy (GSMBE) growth techniques that are most important for the preparation of multiple layer heterostructures for high-speed electronic and optoelectronic devices.

SUMMARY OF RESEARCH:

Initial characterization of the modified Perkin-Elmer 430P MBE system was completed early in 1989. The highest purity p-type GaAs ($N_a \sim 1.5 \times 10^{14} cm^{-3}$ and $\mu_{peak} = 49,000\ cm^2/Vs$ at 15 K) ever reported was grown with the diffusion-pumped MBE system, indicating that the diffusion pump does not significantly contribute to the background carbon concentration.

Since then, work has concentrated on bringing the hydride section of the GSMBE/CBE gas-handling system on line. The growth of InP, $Ga_xIn_{1-x}As$ $Ga_xIn_{1-x}P$ and $Al_xGa_{1-x}P$ using elemental Al, Ga, and In with arsine and phosphine has been investigated. Growth parameters such as substrate temperature, V/III ratio, and hydride gas-cracking temperature have been examined to determine the optimal growth conditions.

The original gas cracker design was modified through a cooperative effort with Union Carbide's Advanced Ceramic Division to obtain a higher cracking efficiency. The modified gas cracker was constructed of a 6-inch long outer pyrolytic boron nitride (PBN) / pyrolytic graphite heater tube and a 12-inch long inner molybdenum tube with PBN and tantalum baffling. The gas cracker cell is capable of operating at temperatures over 1100 °C and has a cracking efficiency higher than 99% at temperatures as low as 750 °C for both AsH_3 and PH_3. The dimer to tetramer ratio for both As and P species is now as high as that of any cracker design currently available. The high dimer to tetramer ratio will be beneficial in the control of the As/P ratio in the growth of the quatenary GaInAsP device structures.

The switching capabilities of the GSMBE/CBE gas-handling system, which are extremely important for the growth of high-quality, abrupt interfaces to be used in future device structures, have been studied. Since typical growth rates for quantum well and superlattice structures are on the order of one micron per hour, which roughly translates to one monolayer per second, switching times on the order of one second or less are desirable for both the column III and column V constituents. Analysis of switching times for both column III solids and column V hydrides has been carried out using a time-resolved residual gas analysis system. Switching times for the column III solids have been determined to be less than one second, but somewhat longer switching times have been observed for the hydrides. Presently, both AsH_3 and PH_3 are injected through the same gas cracker. This led to a significant As/P cross contamination at the heterointerface of the arsenide and phosphide compounds. Modification of the gas panel is underway to eliminate this problem. However, high-quality epitaxial layers of InP,$Ga_xIn_{1-x}P$ and $Al_xGa_{1-x}P$ using a single hydride source, PH_3, have been grown with the GSMBE/CBE system. Some of the important results are summarized as follows:

(1) $Ga_xIn_{1-x}P$ material system:

The $Ga_xIn_{1-x}P$ epitaxial layers were grown directly on (100) on-axis and 2°-off GaAs substrates at temperatures between 460 to 600 °C. The composition required to achieve lattice-matched growth was controlled through the use of *in-situ* reflection high-energy electron diffraction (RHEED) intensity oscillations. Samples grown at both low (near 460 °C) and high (above 580 °C) substrate temperatures exhibited a wide full width at half maximum (FWHM) double crystal x-ray diffraction rocking curve in addition to either weak or no luminescence. The best photoluminescence was achieved for growth temperatures near 500 °C. One sample, grown near the optimum temperature and with a V/III flux ratio of 10, had an extremely narrow emission peak. For this sample, the measured FWHM was 32 meV at 300 K and 6 meV at 22 K. These are the narrowest optical emission line widths ever reported for $Ga_{0.5}In_{0.5}P$ prepared by LPE, MOCVD, or GSMBE. Stimulated emission under pulsed optical excitation at 77 K was also observed for the first time in bulk (1μm thick) $Ga_{0.485}In_{0.515}P$ GSMBE samples grown near optimum conditions.

Spontaneous growth-induced and intentionally introduced long-range ordering phenomena in $Ga_xIn_{1-x}P$ epitaxial layers were studied. Transmission electron microscopy and low temperature cathodoluminescence (CL) techniques were used to examine the microstructure and to determine the band gap energy of the epitaxial layers. The $(GaP)_n/(InP)_n$ short period superlattice (SPS) with each GaP or InP layer about two monolayers thick has been grown by GSMBE on a ternary $Ga_{0.525}In_{0.475}P$ buffer layer which is nearly lattice matched to the GaAs substrate. Comparing the emission photon energies obtained from the low temperature CL spectra of the As-grown and annealed samples, we observed a large band gap narrowing of greater than 150 meV in the SPS, which we attribute to a quasi-CuAu type ordering, i.e., ordering along the [001] direction. We also observed a 37 meV band gap narrowing in the $Ga_{0.525}In_{0.475}P$ buffer layer, which is due to the weak CuPt type ordering along the [111] direction.

(2) $Al_xGa_{1-x}P$ material system:

The initial fundamental study of GSMBE growth of $Al_xGa_{1-x}P$ on (100) GaP has been conducted using elemental Al and Ga solid sources and P_2 generated from PH_3. The results indicate successful $Al_xGa_{1-x}P$ growth can be achieved with the GSMBE growth technique.

The surface structures of epitaxial GaP grown by GSMBE were determined by RHEED. Figure 1 shows the surface structure of the (100) GaP as a function of V/III flux ratio and growth temperature between 575 and 730 °C. Under P_2 stabilization, GaP surfaces exhibited a (2x4) RHEED reconstruction pattern while Ga stabilized surfaces exhibited a (4x2) RHEED pattern. GaP grown within the transition region exhibited a ($\sqrt{19}$x4) RHEED pattern. The minimum V/III flux ratio required to maintain a P_2 stabilized surface between 575 and 660 °C is 2.5, independent of substrate temperature. At temperatures higher than 690 °C, the V/III flux ratio needed to maintain a non-Ga

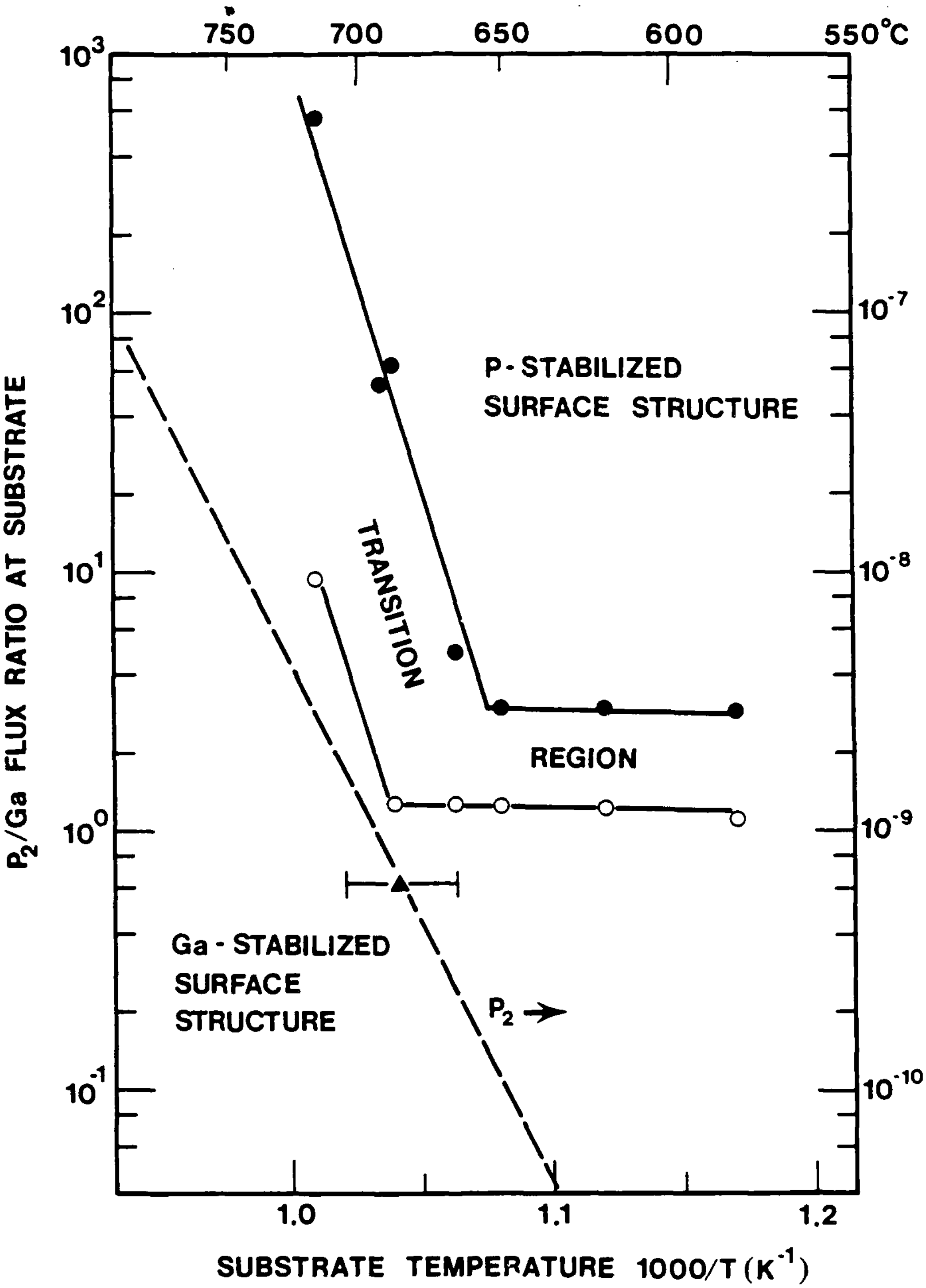

Fig. 1. The surface structures of the (100) GaP as a function of V/III ratio and substrate temperature. The P_2 stabilized surface has a (2x4) pattern, the Ga stabilized has a diffuse (4x2) pattern, and the transition region pattern is ($\sqrt{19}$x4). The energy of the RHEED electron gun is 10 keV. Also plotted is the equilibrium vapor pressure of P_2 along the liquidus curve of the Ga + P system. The triangular point marked at 687 °C is the congruent vaporization temperature of GaP.

stabilized surface increases exponentially with the substrate temperature. The temperature/flux dependent behavior near 690 °C corresponds closely to the congruent sublimation temperature of GaP determined by the Ga + P liquid-solid-vapor phase diagram (687 °C).

The surface structure of $Al_xGa_{1-x}P$, as observed with RHEED, had a V/III flux ratio surface structure dependence that was similar to GaP. For the AlP surface structure, though, a totally different structure was observed. The P_2 stabilized AlP surface structure was (3x2) and this structure was found to be independent of V-III flux ratio when grown between 750 - 830 °C. Owing to system limitations, no metal stabilized or transition region surface structure was ever observed for growth temperatures below 830 °C; however, a transition from C(6x2) to ($\sqrt{19}$x1) was observed at a temperature of 860 °C.

In situ RHEED intensity oscillation was also used to measure the growth rate. At low substrate temperature, this measurement technique was found to be effective at measuring the growth rate for GaP, AlP and its alloy, $Al_xGa_{1-x}P$. The growth rate versus temperature dependence diagram for $Al_xGa_{1-x}P$ was constructed and shown in Figure 2. A small reduction in GaP growth rate was found to occur at ~670 °C and a rapid reduction was found beyond 730 °C. No GaP growth was found to occur beyond 750 °C. For the $Al_{0.35}Ga_{0.65}P$, the reduction in growth rate occurred near 700 °C and was attributed to the desorption of Ga from the growth surface. There was no observed decrease in AlP growth rate for temperatures up to 750 °C. No information was obtained beyond 750 °C due to a sample preparation problem.

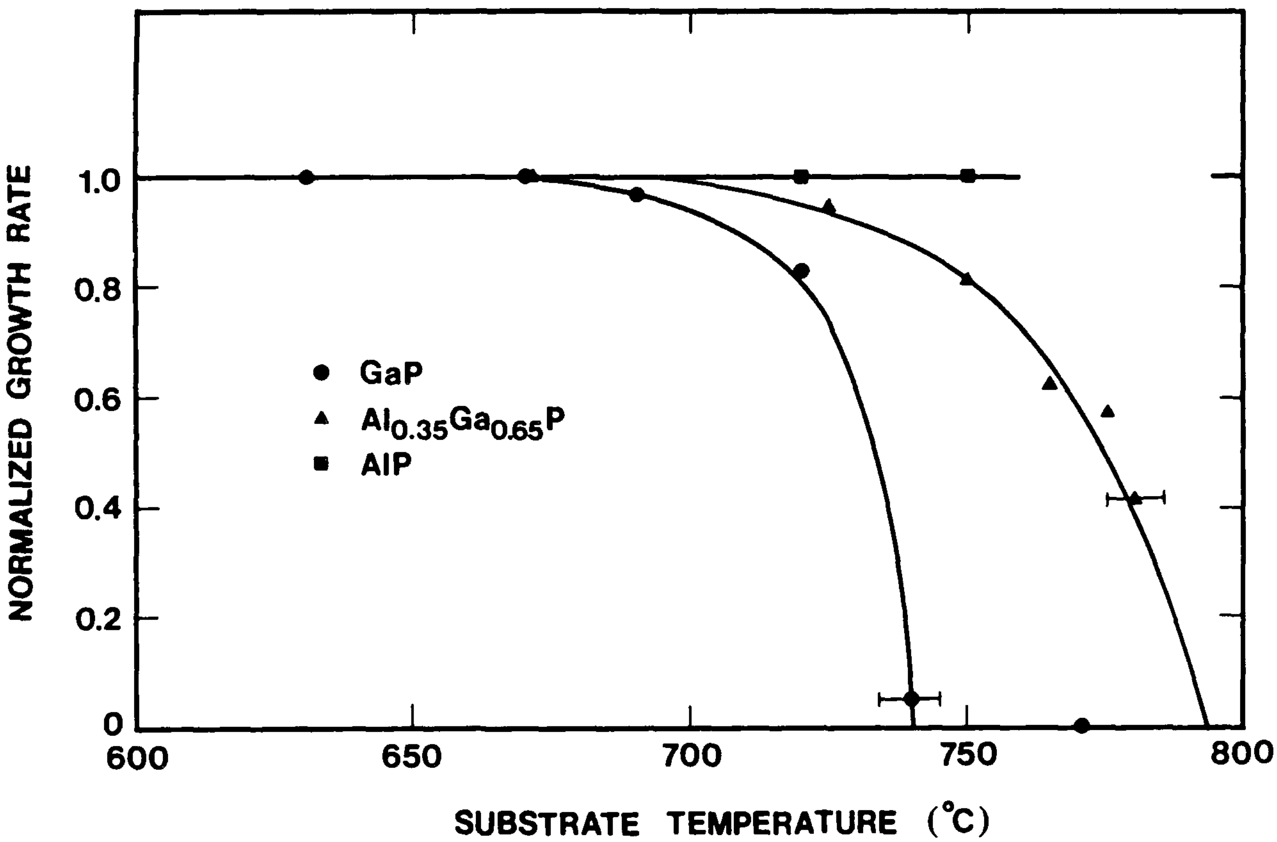

Fig. 2. Normalized growth rate versus substrate temperature for GaP, $Al_{0.35}Ga_{0.65}P$ and AlP. Normalized growth rate is the growth rate at a growth temperature relative to the growth rate below the congruent sublimation temperature.

The doping properties of both GaP and low Al composition AlGaP were determined. In both compounds, Si was a well-behaved, controllable n-type impurity source. The maximum carrier concentration that could be achieved without significant compensation effects in either GaP or $Al_{0.28}Ga_{0.72}P$ was 1.3 x 10^{19} cm^{-3}. This is significantly higher than what can be achieved in the $Al_xGa_{1-x}As$ material system.

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WORK UNIT NUMBER 4

TITLE: Heterostructure Electronic Devices by Metalorganic Chemical Vapor Deposition (MOCVD)

SENIOR INVESTIGATOR:

J. J. Coleman, Research Professor

SCIENTIFIC PERSONNEL AND TITLES:

M. E. Favaro, Research Assistant

SCIENTIFIC OBJECTIVE:

The objective of this program is to extend to electronic devices the enormous impact that metalorganic chemical vapor deposition (MOCVD), as a sophisticated epitaxial growth method, has had on optical device research. This involves fundamental studies of the MOCVD process itself for electronic materials, studies of the electronic properties of heterostructure electronic materials, and studies of devices made from these materials. Two specific areas of interest for this research are: (1) continuation of electronic materials analysis including deep-level transient spectroscopy (DLTS) and Shubnikov-de Haas measurements of quantum well heterostructure and superlattice structures, and (2) development of MOCVD-grown real-space transferred electron devices, the heterostructure hot electron diode (HHED), and other electronic devices.

SUMMARY OF RESEARCH:

In the preceding two years, we have continued work on two real-space transfer devices: the negative resistance field-effect transistor (NERFET) and the charge injection transistor (CHINT). Both devices consist of two conducting layers, a channel with two contacts (source and drain) and a conducting substrate, separated by a potential barrier. The channel is a two-dimensional electron gas at a heterostructure interface that is induced by the application of a positive substrate voltage. With the application of a source-drain electric field (positive drain voltage relative to the source), hot electrons are thermionically emitted over the barrier into the substrate which produces an increase in the substrate current and a concomitant decrease in the drain current. The decrease in the drain current with the associated negative differential resistance in the drain circuit is the basis for the negative resistance field-effect transistor (NERFET). The charge injection transistor (CHINT) is the control of the substrate or injection current by the drain voltage. The initial structure consisted of a n-type GaAs conducting layer, a 2000 Å $Al_{0.45}Ga_{0.55}As$ nearly insulating barrier, and a 2000 Å nominally doped GaAs channel. At room temperature, a drain current peak-to-valley ratio of 2 was measured. A drain current peak-to-valley ratio of 160 at room temperature has been reported in the journals.

In an effort to improve the real-space transfer devices, the GaAs channel was replaced with a thin lattice-mismatched layer (~150 Å) of $In_xGa_{1-x}As$. For sufficiently thin strained-layers, the strain is accommodated elastically and the layer remains commensurate with the substrate. Above a compositionally dependent critical thickness, however, it becomes energetically favorable for the strain layer to relax, forming misfit dislocations. According to the equilibrium mechanical model of Matthews and Blakeslee, a critical thickness of 150 Å corresponds to a maximum In channel concentration of 19%. Our initial results showed an increase in the drain current peak-to-valley ratio with increasing indium concentration in the channel. At an In concentration of 18%, a peak-to-valley ratio of 45 was measured. Our most recent results are for a structure with a 140 Å $In_{0.22}Ga_{0.88}As$ channel. The room temperature drain current peak-to-valley ratio was measured to be over 1000.

In addition, we have experimentally demonstrated the first p-channel negative resistance field-effect transistor. The current-voltage characteristics, measured at low temperature, display negative differential resistance in the drain circuit which is controlled by the substrate voltage. The negative differential resistance is attributed to the real-space transfer of holes. The operation and structure of the p-channel NERFET is analogous to the n-channel $GaAs/Al_{0.45}Ga_{0.55}As$ NERFET. The major differences are the use of a p-type GaAs substrate and the inclusion of an undoped GaAs spacer layer to prevent the outdiffusion of Zn (p-type dopant) from the doped buffer layer into the nearly insulating barrier. Since the undoped GaAs channel and AlGaAs barrier are depleted by the Fermi level pinning at the GaAs surface, a two-dimensional hole gas is induced into a potential well at the GaAs-AlGaAs interface by the application of a negative substrate bias (relative to the source). By applying a negative potential to the drain, holes are heated to energies above their equilibrium values and transfer across the AlGaAs barrier into the substrate. This produces a decrease in the drain current and a concomitant increase in the substrate current. At 26°K, a drain current peak-to-valley ratio of 1.6 was measured.

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WORK UNIT NUMBER 5

TITLE: Scanning Tunneling Microscopy of Semiconductor Devices

SENIOR INVESTIGATORS:

J. R. Tucker, Research Professor
J. W. Lyding, Research Associate Professor

SCIENTIFIC PERSONNEL AND TITLES:

T. C. Shen, Postdoctoral Research Associate

SCIENTIFIC OBJECTIVE:

During the past two years, one of us (JWL) has developed a new design for a scanning tunneling microscope (STM) that possesses several unique features: (1) it is a true temperature-variable instrument capable of operating from liquid He temperatures up to about 420K; (2) it requires little or no vibration isolation and is thus very compact; and (3) the measured thermal drift of <1Å/hour is nearly undetectable. Under our previous JSEP funding period, we have utilized this new STM to directly examine the charge density waves (CDWs) that form in certain classes of quasi one- and two-dimensional conductors below their Peierls transition temperatures.

During the present funding period, we are turning our attention to STM imaging and electronic characterization of semiconductor heterolayers and devices. This requires installing our temperature-variable STM within an ultra-high vacuum chamber and also providing an additional 3-dimensional translation capability to bring atomic-scale interfaces within the lateral scanning range of our STM. These modifications are now nearing completion and we should be ready to begin examining the properties of semiconductor devices on an atomic scale during the coming months. We will focus our initial efforts in the following areas: (1) atomic resolution imaging of AlGaAs heterolayer interfaces, (2) observation of hot electron effects in the presence of strong electric fields, and (3) use of the STM as a tool for producing nanometer scale modifications to semiconductor surfaces, with a goal of eventually creating new types of devices.

SUMMARY OF RESEARCH:

The past year has been largely devoted to building up our local capability to carry out STM research on semiconductor devices. Over the last several years, a substantial body of STM data has been acquired by groups at IBM, Bell Laboratories, and elsewhere on the surface reconstructions of various semiconductors and on submonolayer coverages with various metals. Very little work has thus far appeared, however, on the use of STM to probe device structures. Our aim is to create a unique capability in this area, which should eventually provide unprecedented insights into many device-relevant issues. Here we will discuss briefly and in general terms the technical progress made thus far and some of the experiments we intend to perform. Much detail will be excluded for obvious reasons.

The first requirement for performing STM work on semiconductors is a suitable ultra-high vacuum (UHV) system. We have modified a 25-year-old high vacuum system inherited from C. T. Sah and have used it to a limited extent. Figure 1 is an STM image of InP cleaved in vacuum, showing atomic resolution across the surface chains but not along their length. We were not able to achieve the vacuum levels necessary to work on GaAs or Si with this system, however. Recently, we

STM image of n-InP (110) surface cleaved in UHV.

Sample courtesy of J. J. Coleman's group.

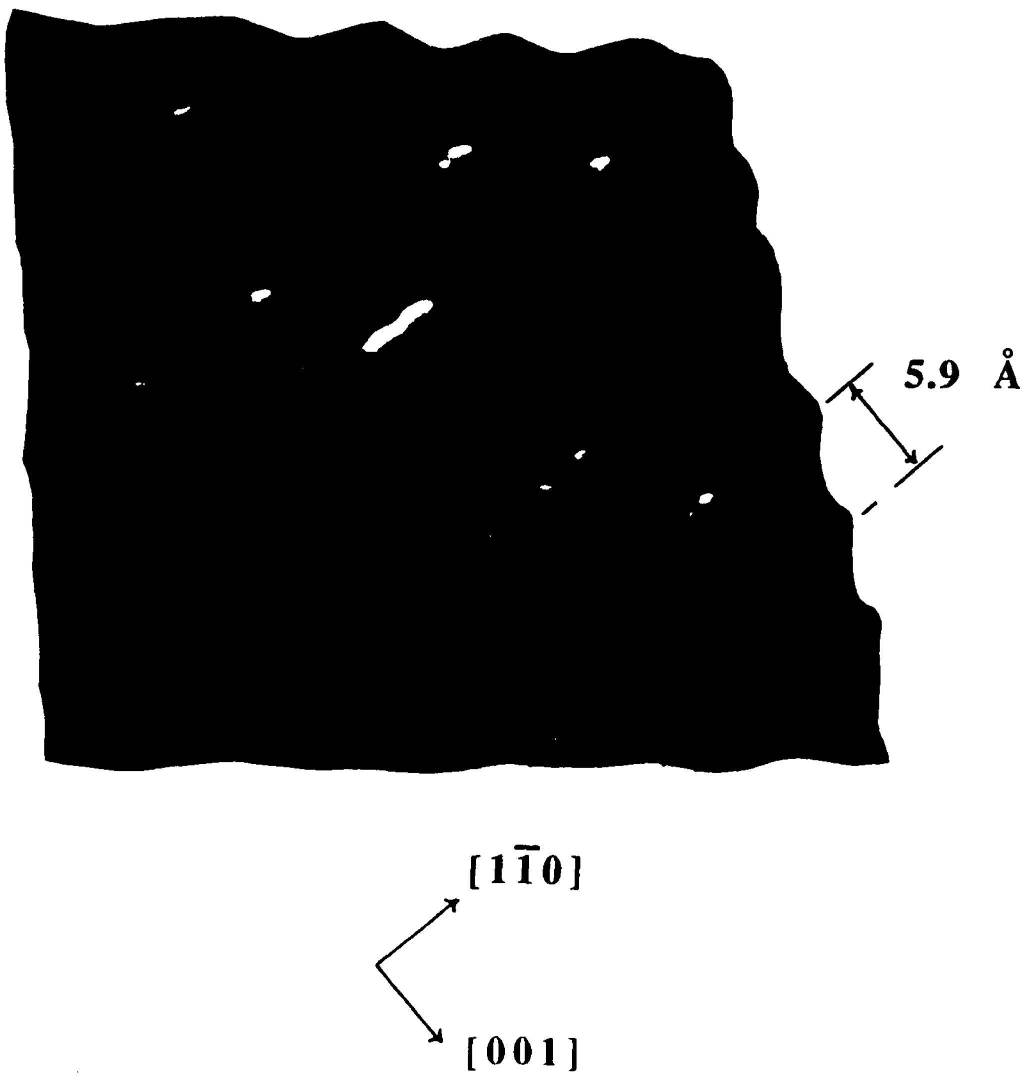

Fig. 1. STM image of n-InP (110) surface cleaved in UHV.

received major funding for a new UHV system through the Beckman Institute. This new system is now under construction. It will comprise three interconnected chambers, with provision for sample preparation and surface characterization, as well as for multiple STMs. This system is expected to be ready for semiconductor device work within the next two or three months.

A unique coarse translation system for our STM has been designed and successfully tested. We are now in the process of incorporating this feature within the STM to be used for device studies. This capability will allow us to position the STM field of view anywhere within an area of roughly $1mm^2$, so that heterolayer boundaries, p-n junctions, and other device features can be easily located.

Over this past year, we have worked on methods to use the STM as a patterning tool. This has included the use of plasma discharge between tip and sample, as well as physical machining of the sample surface with the probe tip. We are now experimenting with these techniques on H-passivated Si surfaces in air. In collaboration with Karl Hess, we have focused on a project to create a new type of quantum interference device operable at high temperatures (77K and above). A preliminary theoretical analysis indicates the feasibility of this device, and we will be working very hard to realize it during the coming year.

Also in collaboration with Karl Hess, we intend to evaluate the capability of our STM to probe hot electron effects. The detection of hot electrons with nanometer scale resolution could potentially provide valuable information in modeling many types of device structures. We will also be collaborating with Nick Holonyak in examining the interfaces of AlGaAs heterolayers with atomic resolution, focusing on effects due to impurity-induced layer disordering.

PUBLICATIONS

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WORK UNIT NUMBER 6

TITLE: Reproducible Semiconductor Laser Frequency Standard: Devices Based on Rare Earth Ions in III-V Materials

SENIOR PRINCIPAL INVESTIGATORS:

J. G. Eden, Research Professor
M. J. Kushner, Research Associate Professor
J. T. Verdeyen, Research Professor

SCIENTIFIC PERSONNEL AND TITLES:

J. Beberman, Research Assistant
R. Fraser, Research Assistant

SCIENTIFIC OBJECTIVE:

To develop narrow linewidth and reproducible laser frequency standards based on stimulated emission of impurity ions in III-V pn junctions.

SUMMARY OF RESEARCH:

I. Introduction

This report of progress on the JSEP unit must be considered in two parts: Part A discusses the progress on the old JSEP Unit 10 entitled "Excited State Chemistry in Gases" for which an established program was in existence and thus there was significant progress. The new JSEP program represents a considerable deviation from past history and has only been operational for ~6 months; hence, we are still on a learning curve for that work. Consequently, we report progress under the former project in Section II and that of the new unit in Section III.

II. Progress on "Excited State Chemistry in Gases"

A. Modulation Effects in Plasma Processing

As has been reported previously, we have found a significant change in the characteristics of plasma deposited amorphous silicon when the RF source is 100% modulated. In particular, the following statements have been proven under JSEP support:

(1) The bandgap is reduced [3].

(2) The deposition rate is enhanced [4].

(3) The electron density is enhanced [4].

(4) The negative ion flux to the surfaces is enhanced [1].

(5) The particulate formation (or "dust") is dramatically reduced [2].

The first three items apply to the deposition type of discharges, whereas the last three appear to be true in all plasma processing discharges [2,5,6]. It should be emphasized that all are most desirable and are accomplished by the simple expedient of turning the discharge on and off at an audio rate

(~100-1 kHz). It appears that all phenomena are interconnected and find a common denominator with the presence of negative ions. For instance, it is our hypothesis that the negative ions, being confined by the sheaths, act as a nucleation site for the formation of macrosized particulates. By turning off the discharge, the negative ions disappear and "dust" does not form. The effect has also been seen in etching discharges [5] and by the Japanese [6].

B. Production of Column IIIB Metal Ions

During the first six months of this year, detailed studies of the photoionization of indium monoiodide (InI) to yield singly charged In ions were completed. The primary motivation behind these experiments was (and is) the development of efficient optical approaches to producing Column IIIB metal ions for implantation or III-V epitaxial film growth. Existing ion production techniques are inefficient and, more importantly, nonselective. Also, the latter often require expensive mass selection hardware.

Various paths to producing In^+ ions were explored by laser-induced fluorescence and multiphoton spectroscopy. Figure 1 is a partial energy level diagram for InI and illustrates one of the channels that is available in the violet (λ~428nm). Although the lowest excited states of InI are stable, the higher-lying levels are dissociative, which provides a convenient pathway for atomic ion formation. Figure 2 demonstrates that this is, indeed, the result. This figure shows the relative number of indium ions that is collected (in a Geiger-Müller configuration) as the dye laser wavelength is scanned. Most, if not all, of the indicated resonances correlate with Rydberg states of the **atom**, which indicates that the diatomic first absorbs two photons and dissociates. Subsequently, the atom absorbs two more photons and is ionized.

The results of this work were that:

(1) The intermediate InI molecular states (AO^+ and B1) were thoroughly characterized spectroscopically;

(2) The high-lying ($n > 30$) Rydberg states of In were also observed (several for the first time) and their existence is of more than academic interest—they serve to strongly enhance the production of In^+ ions as indicated in Figure 2;

(3) The efficient production of In ions with low laser pulse energies (mJ) was demonstrated.

Certainly, similar processes are available for the other Column IIIB metals (Al and Ga) and the low pulse energies required to selectively ionize the atom indicate that tunable, frequency-doubled diode lasers will, in the near future, make this an **inexpensive** as well as selective source of ions.

III. Progress on "Development of a Monolithically Integrated Frequency Standard"

The main thrust of the work proposed for the new JSEP unit was to devise a means to produce a transportable frequency standard using semiconductor laser technology. At the time of the proposal, we felt that there would be a good chance of incorporating a reference standard "ion" into the junction region and either make this lase or use it as a saturable absorber. Given the fact that the transitions in the rare earth ions (Er^{3+}, Nd^{3+}, etc.) are more or less independent of the host suggests that these impurities could serve as a "reference" wavelength. The fact that Tsang and Logan succeeded in doping InGaAsP with erbium and achieved lasing at 1.532 μm [7], followed by the French [8] and Japanese [9], gave considerable impetus to this approach. It is still a viable one, but we also feel that there is an easier approach with less risk and using simpler technology.

In our opinion, there is no intrinsic practical virtue in incorporating the impurity ion or standard in the junction; rather, the goal should be that the configuration should be capable of monolithic integration. Thus, if a doped material can be fabricated on a chip, then one has the monolithic frequency standard.

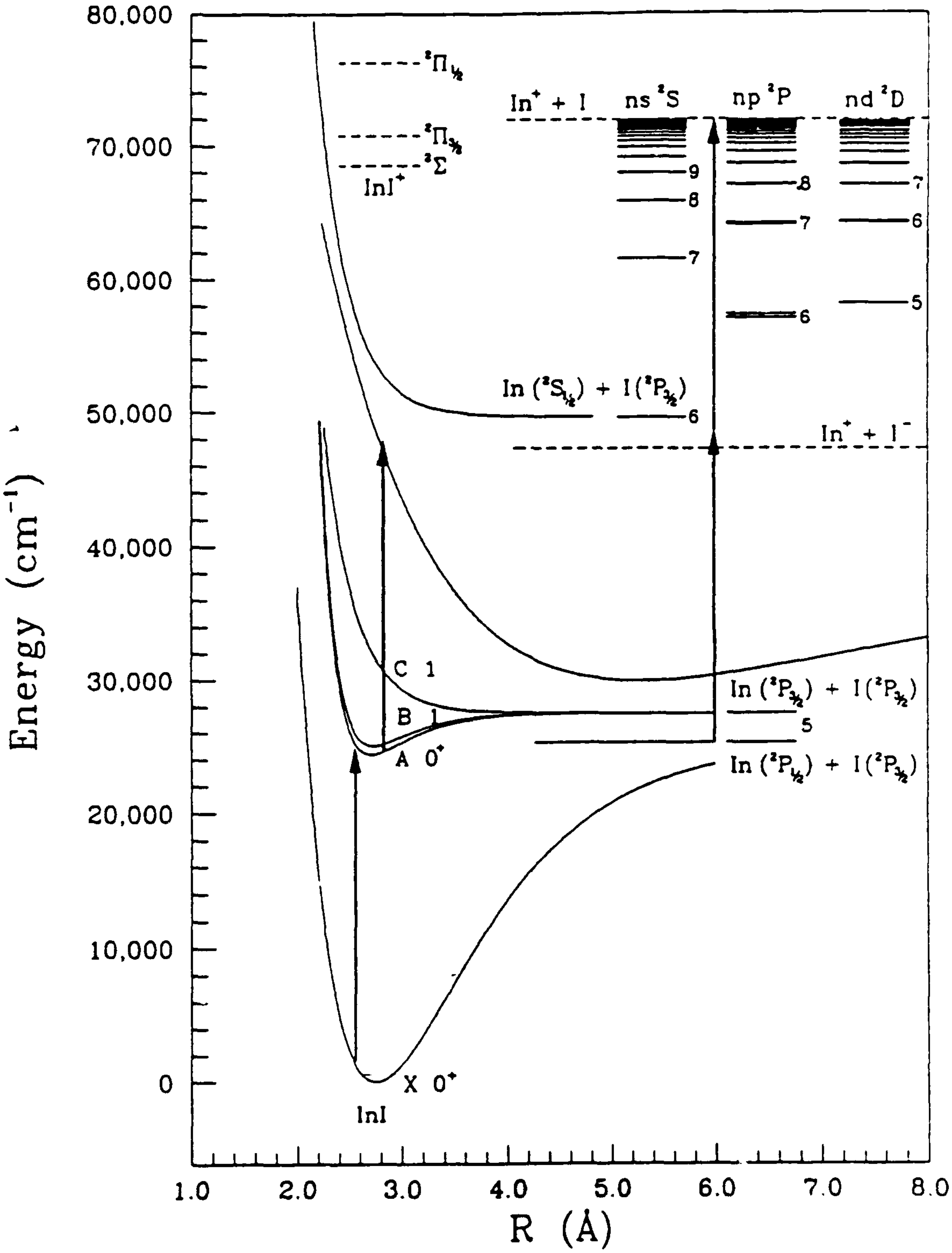

Fig. 1. Partial energy level diagram for indium monoiodide showing ionization pathways when the dye laser is turned to 428.37 nm.

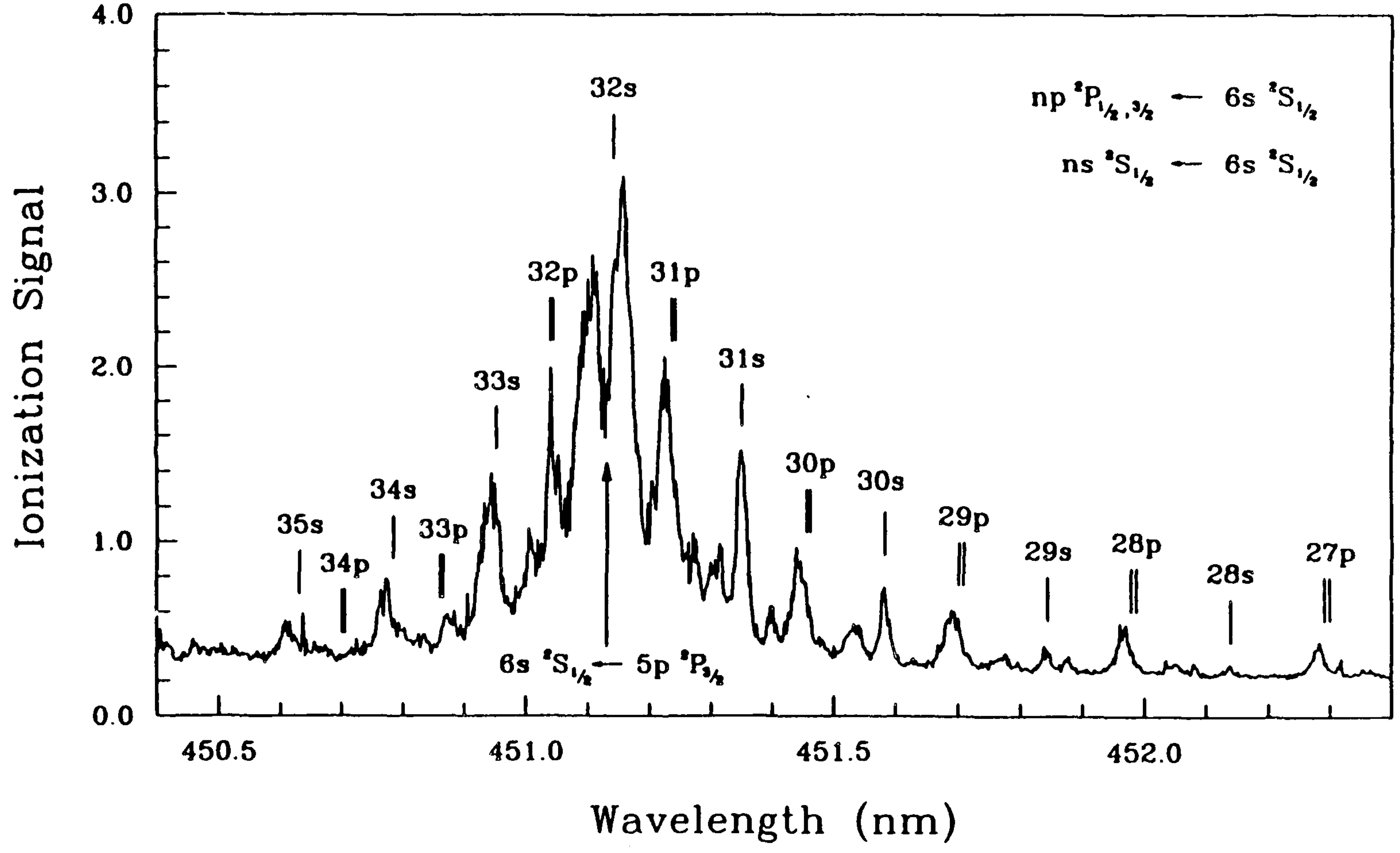

Fig. 2. Ionization spectrum of InI in the range 450.5 - 452.3 nm.

Thus, our immediate approach is sketched in the diagram shown below and uses some of the technology developed by Professor Coleman's group involving patterned substrates. The key point is that his group has demonstrated that one can produce a laser array which is many times wider than it is long with significant power and no concern with ASE [10]. Given the experimental existence proof of such a laser array, it is then a simple extension of standard optical pumping techniques and conventional semiconductor etching, masking, lase ablation, and oxide-nitride growth to achieve a monolithic frequency standard.

This, we feel, is a much more straightforward task than that of incorporating these ions directly into the junction. That goal is still of interest, but the above approach promises a much faster yield. The approach is sketched in Figure 3 below where the proposed monolithic structure is envisioned.

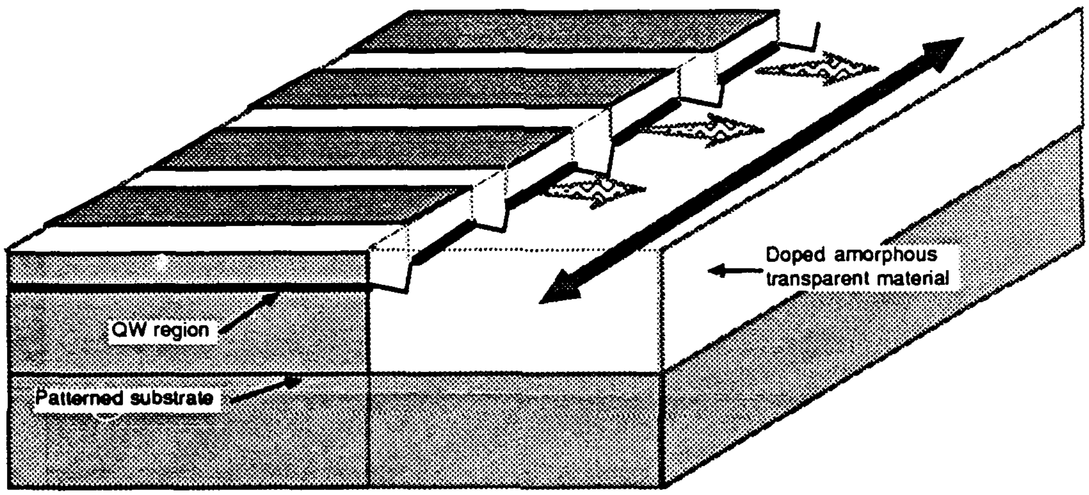

Fig. 3. A sketch of the integrated laser. The doped material may function as a laser or as a saturable absorber.

Toward that end, we are developing the capability of growing the optically transparent insulator host and doping it with the rare earths. Our first approach has been to use active nitrogen plus silane to produce high quality Si_3N_4. To dope it, we plan to use laser ablation of either a high purity metal source or of a doped crystal. The researchers working in high T_c superconductors have demonstrated the highest quality films using this technique. Amazingly, laser ablation permits one to transport a rather complex structure from one body to another and maintain stoichiometric ratios. Hence, it may well be that one can deposit amorphous YAG from a source directly onto the semiconductor.

Professor Eden is exploring another approach along these same lines. The first step is to evaluate in detail Nd:YAG platelet lasers pumped by GaAs diodes. This scheme, recently demonstrated by Aram Mooradian [11] at MIT, entails pumping a several hundred μm thick platelet of Nd:YAG with a < 500 mW GaAs diode laser. Since the threshold pumping powers for these devices are low (< 200 mW), it is ideally suited as an oscillator for injection into a III-V "slave" amplifier. Also, the small active volumes required do make it compatible with OEIC technology. Presently, we are duplicating Mooradian's [11] and Scarl's [12] experiments with YAG or YALO as the rare earth host, respectively, in order to determine threshold accurately as a function of rare earth doping. The next step is to lock an InGaAsP amplifier onto the 1.06 μm transition and, in the future, we expect to move to a similar scheme with Er^{3+}:YAG, YALO or YLF at 1.54 μm. Once this has been accomplished, we will investigate laser ablation as a technique for depositing stoichiometric and crystalline YAG films onto GaAs substrates.

C. Femtosecond Facility

In the past six months, we have also been constructing a femtosecond laser system that we expect will be extremely valuable, not only for this JSEP unit, but also for other projects within the JSEP program. Our initial goal for this system is, as discussed in the original proposal to JSEP one year ago, to determine by time-resolved spectroscopy the manner in which energy is transferred from a III-V semiconductor, such as GaAs, to the rare earth ion. This information is essential to intelligently designing a rare earth/III-V host diode or laser as it will reveal, in real time, the relative populations of the semiconductor's conduction band as well as the ion's upper state (4f) number density.

The femtosecond oscillator (colliding pulse mode-locked system) has been operational for one month and we are in the process of completing an autocorrelator for accurately measuring the pulse width. However, several measurements made with this system show that the mode-locked pulses have widths < 300 fs. Once completed, this ultrashort pulse laser system will be made available to other researchers for performing real time measurements of the bandwidth of detectors and other devices of interest to the JSEP program.

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WORK UNIT NUMBER 7

TITLE: Electronic and Transport Properties of Ultra-Low-Dimensional Semiconductor Structures

SENIOR INVESTIGATORS:

I. Adesida, Research Assistant Professor
J. Kolodzey, Research Assistant Professor
J. P. Leburton, Research Associate Professor

SCIENTIFIC PERSONNEL AND TITLES:

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D. Jovanovich, Research Assistant
K. Nummila, Research Assistant

SCIENTIFIC OBJECTIVE:

This work unit explores the potential of ultra-low-dimensional semiconductor structures for electronic and optical device applications. The emphasis is placed on fast transients and the research is concerned with the conception, design, and investigation of nonconventional devices characterized by extreme quantization of the electronic system.

Our method involves an integrated theoretical and experimental approach including various technological components from material growth, processing, and testing to numerical simulation of nanostructures. In addition, we are conducting a fundamental investigation of new physical effects in ultra-low-dimensional systems.

SUMMARY OF RESEARCH:

I. Growth of High-Mobility Materials and Structures by MBE

High-mobility materials and structures will make extreme electron confinement effects more evident, as they will be used in the fabrication of one-dimensional devices. We are using two approaches to achieve high mobilities:

(a) High-purity MBE source materials

We have consulted with Drs. A. Y. Cho and N. Chand of AT&T Bell Laboratories and have concluded that the purity of the As source significantly affects the mobility of GaAs layers. We have discussed this need with experts from UMC-Furukawa Corporation and have obtained from them an experimental grade of As having ultra high purity: 7Nines5 (99.999995%). After discussions with several manufacturers of As effusion cells, we obtained from EPI Corporation a special type of As bulk evaporator and cracker cell that has the unique feature of using only Ta metal in contact with the As. Using this method, we obtained bulk GaAs films having a mobility of 120,000 $cm^2-V^{-1}-s^{-1}$ at 77 K, a respectable value.

(b) Atomic planar or delta (δ) doping

We are exploring δ-doping as a technique to obtain both high mobilities and high carrier concentrations. The confinement of dopant atoms to a single atomic plane reduces spatial variations in the Coulomb potential and decreases ionized impurity scattering. The restriction of dopants to Group-III atom sites increases the effective doping concentration by reducing self-compensation. For a modulation-doped structure of pseudomorphic $Ga_{0.8}In_{0.2}As$ grown on GaAs, we obtained a record electron mobility of 118,600 cm^2–$V^{-1}s^{-1}$. We are evaluating both p-type and n-type δ-doped layers using Hall effect measurements. Our plan is to process these layers into one-dimensional transistors with lateral confinement using e-beam lithography.

II. Fabrication

(a) Nanostructure fabrication

We have developed a selective reactive ion etching (SRIE) process for GaAs on AlGaAs using $SiCl_4/SiF_4$ plasma. A selectivity of 350:1 for GaAs/AlGaAs has been achieved at low power. This process has been applied to the fabrication of GaAs/AlGaAs and GaAs/AlGaAs/InGaAs modulation doped field effect transistors (MODFETs). The dc and rf characteristics of the reactive-ion-etched and wet-etched devices were identical, which indicates that no damage was induced in the device heterostructures by the SRIE process. We have developed nanolithography on a computer-controlled scanning electron microscope using a bilayer PMMA resist approach to achieve 30 nm isolated lines and 60 nm-period gratings. This has been used along with a methane-based etching process to produce nanostructures in InP and related materials. Current efforts are directed toward the installation of a chemically assisted ion beam etching (CAIBE) equipment donated by Varian Associates. The processes outlined here will be applied to the fabrication of quantum effect devices beginning with a quantum wire channel FET.

(b) Device fabrication

We have fabricated high-performance 200 nm gate-length MODFETs in pseudomorphic GaAs/AlGaAs/InGaAs and lattice-matched InAlAs/InGaAs materials. The devices in the pseudomorphic material exhibited an f_T of 76 GHz while the devices in the lattice-matched material exhibited a record f_T of 170 GHz. Currently, MODFETs with gate-lengths as small as 30 nm are being fabricated to investigate quantum transport in FET channels at room and cryogenic temperatures. Low temperature measurements (down to 4 K) on these devices and the quantum wire FETs will be conducted in the Material Research Laboratory where a new liquid helium dewar equipped with a magnet is being purchased.

III. Device Characterization

(a) Transport in two-dimensional devices

The transport mechanisms underlying device operation can be distinguished by their temperature dependence. To understand the limitations of two-dimensional pseudomorphic AlGaAs/GaInAs MODFETs, we have evaluated their frequency response at 300 K and 77 K, as a function of device gate length. We have found that for longer gate lengths from 0.8 to 1.7 μm, the current gain cutoff frequency doubles by cooling the devices to 77 K. For shorter gate lengths from 0.25 to 0.4 μm, the cutoff frequency increases by about 20% with cooling. The amounts of increase are consistent with published values of drift velocity versus temperature but are far less than the factor of ten increases in mobility we measured by cooling to 77 K. We conclude that carrier velocity, rather than mobility, is controlling the frequency response of these MODFETs.

IV. Transport Properties and Simulation of Quantum-Wire Structures

During this last year progress in fundamental transport properties of one-dimensional (1-D) structures has been realized in the following directions:

(a) We have generalized our model of Resonant Inter-Subband (polar) Optical Phonon Scattering (RISOPS) and have investigated high-order resonances n ($n\Delta E$ = optical phonon energy with ΔE being the 1-D subband spacing) by taking into account appropriate broadening in the density of states (DOS) due to the electron-phonon interaction. Monte-Carlo simulations were performed at 150 K and 300 K for a range of confinement varying from the 1st to the 3d order resonance and showed significant differences in the carrier velocity characteristics. Optimum resonance conditions are realized at 150 K as a result of a trade-off between sharper scattering rates corresponding to a reduction in the DOS broadening and the decreasing inter-subband phonon absorption rates responsible for RISOPS; structures at different resonance orders corresponding to minima in the velocity are clearly visible in the characteristic (see Figure 1). At 300 K the velocity minima have considerably smoothened and shifted from the resonances, mainly because of the large DOS broadening in the absorption rates which weakens RISOPS.

As previously established, population inversion between nonresonant subbands is found to occur under RISOPS conditions. However, as a particular feature of the parabolic confining potential, this effect is quenched at room temperature because of the strong intersubband phonon absorption rate, which distributes more homogeneously the carrier population between the equally spaced upper subbands of the harmonic oscillator-like energy spectrum. This homogeneous carrier redistribution reduces the effect of the population inversion.

(b) We have also carried out a gain analysis for far infra-red (FIR) stimulated emission resulting from population inversion under RISOPS conditions and have shown promising performance with a theoretical gain of the order of 100-1000 cm^{-1} for FIR lasers based on this effect. The recent approaches for fabricating large arrays of dense and regular quantum wire structures directly from growth on patterned GaAs substrates by MBE [15] or MOCVD [16] seem to be particularly suited for evidencing FIR-stimulated emission.

(c) Finally, we have clarified the transport nonlinearities arising at low electric fields in 1-D systems in the presence of optic phonon scattering. We have firmly established the limitations of the linear response approximation for these systems characterized by the absence of angular randomization and short range inter-carrier interaction.

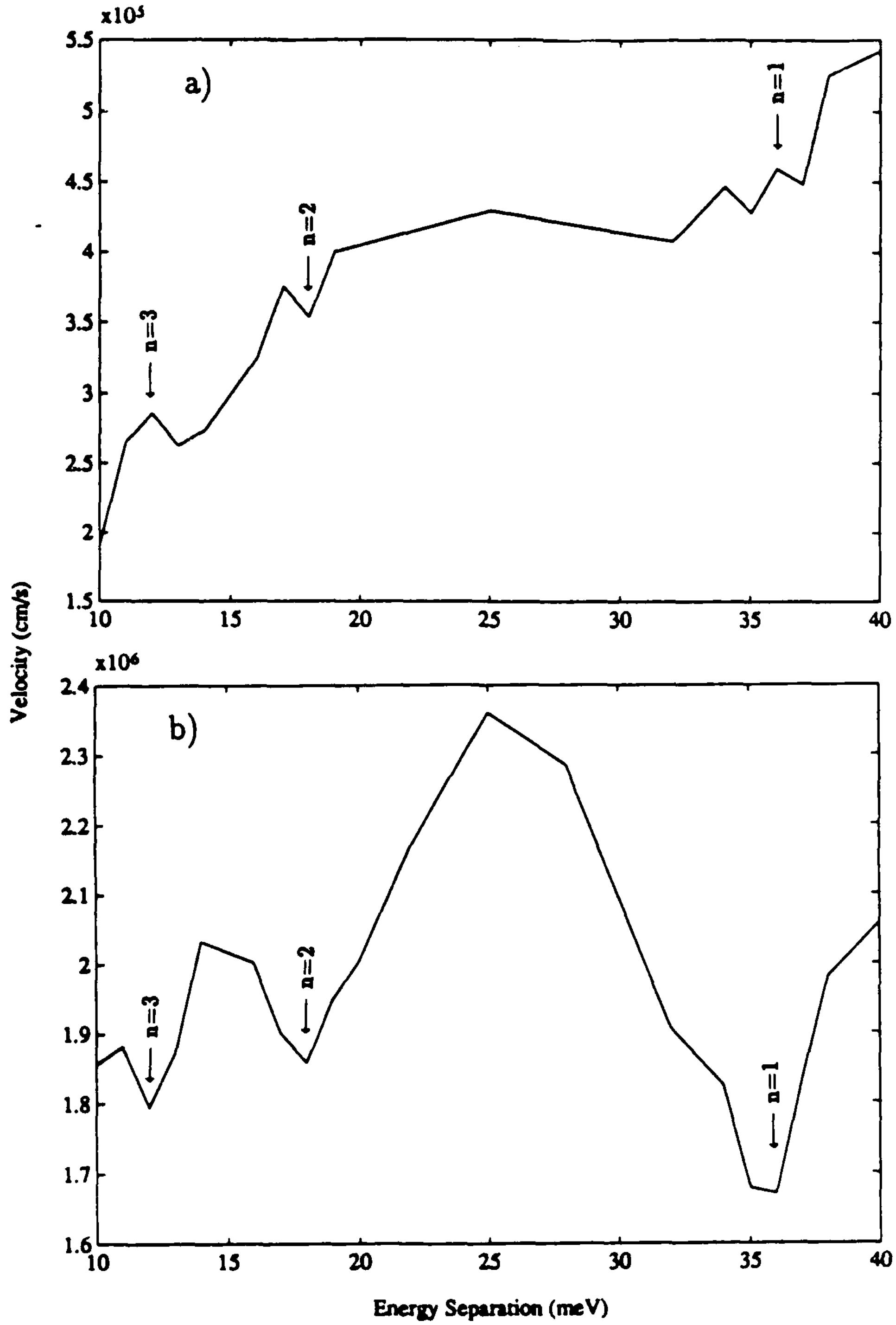

Fig. 1. Electron velocity as a function of subband energy separation, $\hbar\omega$, at (a) T=300K with a DOS broadening $\delta\ E_{ph}$=2.3meV and at (b) T=150K with $\delta\ E_{ph}$=2.6meV. Both sets of data are taken for a quantum wire system consisting of a parabolic confining potential with zero-point energy $\hbar\omega/2$ and a 150Å wide quantum well in a longitudinal driving field of 50 V/cm.

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WORK UNIT NUMBER 8

TITLE: Optimum Interconnect Design for High-Speed Digital Applications

SENIOR INVESTIGATORS:

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J. Schutt-Aine, Research Assistant Professor

SCIENTIFIC PERSONNEL AND TITLES:

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R. Baca, Fellow
W. Becker, Graduate Student
W. S. Chi, Graduate Student
P. Harms, Graduate Student
S. Kosanovich, Graduate Student
A. Kouki, Graduate Student
J. F. Lee, Visiting Postdoctoral Student
D. McNay, Graduate Student
R. Palandech, Fellow
G. Wilkins, Fellow

SCIENTIFIC OBJECTIVE:

The objective of this effort is to develop electromagnetic modeling of electronic packages with applications in digital and microwave circuits.

SUMMARY OF RESEARCH:

There are fivè major aspects of research being pursued in the area of electronic packaging. These are: (a) direct time domain field modeling and extraction of circuit parameters; (b) frequency domain modeling of multi-line etches with discontinuities; (c) development of techniques for predicting crosstalk and signal distortion in multiconductor transmission lines terminated by active devices; (d) development of new transmission line configurations with low crosstalk and dispersion; and (e) experimental characterization of electronic packages. The direct time domain method for solving electric and magnetic fields in packaging configurations is becoming increasingly attractive as a means for deriving equivalent circuits and scattering matrices for these packages. We are investigating three different time domain methods: the Finite Difference Time Domain (FDTD) method, the Transmission Line Matrix (TLM) method, and the Bergeron method for solving the field modeling problem on the Cray-XMP and the CM-2 connect.

In parallel with the time domain effort, we are carrying out research in the frequency domain and investigating integral equation methods for computing the capacitance and inductance matrices of multiconductor lines and discontinuities in these lines, e.g., bends. We are developing numerical techniques for efficient derivation of these models in order to prove them useful as tools for CAD design of circuit boards.

The circuit models for discontinuities and the [C] and [L] matrices for multiconductor lines are needed for predicting the signal degradation and crosstalk. We are developing algorithms for simulating the signal propagation in multiconductor transmission lines that are terminated by active devices using a combination of distributed and lumped circuit models.

We are developing a new type of transmission line configuration that may be useful both in packaging configurations and in measurement circuits because of its promise for low crosstalk as well as dispersion properties. A prototype of this line has been designed and tested and the preliminary results appear to be promising.

Accurate measurement and characterization of electrical properties of electronic packages play a very important role in successful design of these packages. The experimental results also serve to validate the theoretical models being developed for the packages. We have been investigating techniques for accurate experimental measurement as well as for de-embedding the experimental data and applying putting these methods to test by making measurements on some representative circuit boards and components, e.g., chip carriers.

PUBLICATIONS

JSEP-SPONSORED PUBLICATIONS:

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WORK UNIT NUMBER 9

TITLE: High-Performance Computer Architectures

SENIOR INVESTIGATORS:

J. H. Patel, Research Professor
W. W. Hwu, Research Assistant Professor

SCIENTIFIC PERSONNEL AND TITLES:

J. Fu, Graduate Research Assistant
S. Anik, Graduate Research Assistant

SCIENTIFIC OBJECTIVE:

This unit seeks to develop, model, and analyze efficient computer architectures that will exploit semiconductor technology to deliver high performance for important applications. High-density technologies such as CMOS VLSI have provided high-performance, low-cost computation elements for parallel processing systems. To achieve high performance, the nature of important applications must be characterized to provide insights into how compilation and hardware techniques affect the performance of parallel processing systems. We will address two major aspects: processor/system architectures and memory architectures. In both cases, we will develop integrated architecture, compilation, and analysis methodologies to achieve high performance for important military, scientific, and engineering applications.

SUMMARY OF RESEARCH:

Processor/System Architectures

We have developed a hierarchical method to quantify the impact of architectural support for task management on the performance of parallel processing systems. The thrust is to base our study on real parallel application programs whose importance and execution time justify their parallelization. The PERFECT Club benchmark suite satisfies this requirement in that the programs solve important problems in real application domains and the inputs are collected from the real usage of these programs. The programs in the PERFECT Club are described in Table 1.

Our method starts with parallelizing the benchmark programs with the CEDAR parallelizing compiler developed at the Center for Supercomputer Research and Development of the University of Illinois. The parallelization is expressed in the form of DO-ALL loops, DO-ACROSS loops, mutual exclusion, and data synchronization. It is straighforward to identify high-level task management requests by examining the parallelized source code. By inserting probes into the source code, we can compile and execute the programs to take high-level event traces that record the dynamic task management requests and shared variable accesses.

The second step is to define the low-level system primitives for synchronization. The high-level task management functions are expressed with these low-level primitives. With this information, we translate each high-level event trace into a low-level parallel execution trace that consists of synchronization primitives and shared memory accesses. In this step, the effects of special synchronization primitives and task management techniques are taken into account.

TABLE 1

PERFECT Club Programs

Program	Application	Lines of Source	Sponsor
ADM	Air Pollution	6142	IBM
ARC3D	Computational Fluid Dynamics	3605	Cray
BDNA	Nucleic Acid Simulation	3962	IBM
DYFESM	Structural Dynamics	7599	Illinois
FLO52Q	Computational Fluid	2250	Princeton
MDG	Liquid Water Simulation	1231	IBM
MG3D	Seismic Migration	2754	Cray
OCEAN	Computational Fluid Dynamics	4215	Princeton
QCD	Quantum Chromodynamics	2342	CalTech
SPEC77	Weather Simulation	3880	Illinois
SPICE	Circuit Simulation	18504	Illinois
TRACK	Missile Tracking	3370	CalTech
TRFD	Quantum Mechanics	479	IBM

The third step is to feed the low-level parallel execution trace into a parallel system simulator. The simulator models the processor, interconnect, and memory system. In this step, the effects of special implementation supports such as combining, synchronization memory, event ordering, and topology of interconnect are taken into account. The simulation extracts system performance measures such as processor utilization, interconnect conflicts, memory conflicts, and speedup over the sequential version of the program.

The most challenging part of the project is to design the experiments to quantify the effect of task management schemes, system synchronization primitives, and the system implementation methods. One challenge arises from the fact that these design choices span an extremely large design space. Another challenge is that the design choices are coupled with each other. For example, to be effective a special system synchronization primitive often requires special system implementation methods. We are investigating methods to derive conclusive results for the design of hardware and software for parallel processing systems.

Memory Architectures

We have continued to develop our methodology for low cost trace-driven simulation for evaluating cache memory systems. Our methodology samples the execution trace of programs and uses the sampled trace for trace-driven simulation. Experiments have shown that the sampled trace is a good representation of the complete program trace. Furthermore, we have shown that the sampled trace can be used to obtain accurate estimates of cache performance at a fraction of the time and disk storage costs for full trace simulation. Since any realistic program with a realistic input data set can generate billions of references, trace sampling is an effective approach to trace-driven simulation with real programs. We have applied our methodology to various cache organizations using a variety of general purpose programs and numerical applications.

The sampled trace-driven simulation methodology is currently being used in a study of memory organizations for vector processor systems. We have studied the cache performance of several numerical applications taken from the PERFECT Club, a well-known collection of benchmarks. Specifically we have looked at the performance of various unified and split scalar-vector cache organizations for a uni-processor. Our results indicate that while cache memories are beneficial in a vector environment, the presence of long stride vector accesses can result in dramatic cache behavior. Furthermore, the selection of cache parameters, such as the cache block size, for such a cache design is more difficult than for a cache for nonvectorized workloads. For instance, we have found that a particular block size that results in the best performance for one vectorized program may result in the worst performance for another vectorized program. We are currently studying trade-offs in accessing and caching long stride vectors. Our results also indicate that a unified cache is preferable to a split scalar-vector cache. This is due to the poor performance of the separate vector cache when compared with the vector performance of a larger unified cache and the high rate of interference between the scalar and vector reference streams in the split cache system.

An extension to the above work is memory organizations for multiprocessors and, in particular, vector multiprocessors. While current vector multiprocessors do not generally feature vector caching, caches are an effective approach to designing a memory system for multiprocessors. Caches in a multiprocessor system not only reduce the average memory access latency but also each processor's memory interconnection bandwidth requirement. As the speed of individual processors and the number of processors increase in multiprocessor systems, caches may be the only feasible cost effective solution to meeting the memory bandwidth requirements. However, the design of a vector cache in a multiprocessor system requires careful trade-offs in the selection of the cache parameters. For instance, a large cache block size is good for stride one vector accesses due to its spatial locality, but large block transfers between the caches and the memory may result in periods of memory interconnect saturation, particularly during burst vector accesses. Furthermore, our early results indicate that large block sizes will result in a high rate of block invalidations when a write-invalidate cache coherence protocol is used. We intend to continue the study of multiprocessor memory systems using the sampled trace-driven simulation methodology.

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WORK UNIT NUMBER 10

TITLE: Fault-Tolerant Parallel Computer Systems

SENIOR INVESTIGATORS:

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W. K. Fuchs, Research Associate Professor
R. Iyer, Research Professor

SCIENTIFIC PERSONNEL AND TITLES:

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C. C. Li, Research Assistant
D. Tang, Research Assistant

SCIENTIFIC OBJECTIVE:

This unit will explore concepts in reliable computing that will provide an understanding of the basic principles in design and analysis of reliable VLSI-based parallel computer architectures. As advances in integrated circuit technology continue, the resulting complexity in the systems developed require new approaches for realizing reliable and fault-tolerant systems. There is an increasing need for systems that will continue to function under a variety of workload environments and failure conditions. We have identified three issues that require particular attention from both technology and systems viewpoints. Basic research will be performed in the specific areas of reconfiguration for fault tolerance in parallel architectures, recovery from errors in parallel architectures, and the development of realistic models to describe the dependability of parallel computer systems.

PROGRESS: April 1, 1989 - March 31, 1990

Reconfigurable Parallel Architectures

In the past year, we have initiated research into the investigation of hardware- and software-based reconfiguration strategies for hypercube-based parallel architectures. The studies have resulted in three schemes for reconfiguration, two in hardware and one in software [1]. The hardware schemes use cost-effective embeddings of spare processors in the system with optimal reconfiguration and rerouting strategies. The software scheme requires no hardware modification and is based on the notion of reconfiguration using virtual processors. We have also investigated two rerouting strategies for hypercubes under faults [2]. Both are table-driven strategies. We have proposed two table-filling algorithms, one centralized and another distributed.

The future work is to develop an experimental environment to study reconfiguration and rerouting strategies, and load balancing under failures on an actual Intel iPSC/2 hypercube. We also plan to investigate and evaluate the cost/performance trade-offs in various schemes using analysis and simulation [3]. We are planning to use a recently developed trace-gathering system for parallel applications on the hypercube to generate statistics on computational and communication requirements to evaluate the performance degradation of actual parallel applications.

Error Recovery in Parallel Architectures

In the area of error recovery in parallel architectures, we have made specific progress concerning the use of compiler technology in determining checkpoint placement and checkpoint contents [4,5], and recovery through graceful degradation [6].

We have developed a compiler-based approach to generating efficient checkpoints for process recovery [4,5]. Our approach to checkpointing is programmer, operating system, and hardware transparent. Compile-time information is exploited to maintain the desired checkpoint interval and to reduce the size of checkpoints. Compiler-generated sparse potential checkpoint code is used to maintain the desired checkpoint interval. Adaptive checkpointing has been developed to reduce the size of checkpoints by exploiting potentially large variations in memory usage. A training technique is used in selecting low-cost, high-coverage potential checkpoints. Since this potential checkpoint selection problem is NP-complete, a heuristic algorithm has been developed to obtain a quick suboptimal solution. These compiler-assisted checkpointing techniques have been implemented in a modified version of the GNU C (GCC) compiler.

We have also developed an incremental checkpointing scheme for rollback recovery that determines at compile time the information to be checkpointed. A checkpoint is either a major checkpoint, which saves the entire state space, or a minor checkpoint, which saves the difference between the current and the previous state spaces. The compiler analyzes the program to obtain the modified live variables between any pair of potential checkpoints and constructs static maps for the checkpoint subroutine to establish the minor checkpoints.

Our final area of progress in the last twelve months has been the development of a data redistribution approach to graceful degradation for hypercube multiprocessors [6]. CPU-bound hypercube programs using the described second-order parametrized data distribution technique can run on a group of cubes of any size to achieve graceful degradation without recompilation. A transmission mechanism has been designed to switch the performance of a second-order parametrized data distribution hypercube program to that of a corresponding first-order program when the latter is superior. A package of procedures has been implemented on the Intel iPSC/2 hypercube to support the approach.

Modeling and Measurement of Computer System Dependability

In order to extract models to quantify the dependability aspects of a complex system in conjunction with its operating environment, we concentrated on the dependability measurement and modeling for a distributed environment in the last year. We collected a set of real error data from a 7-machine DEC VAX cluster multicomputer system for approximately eight months of operation. Based on the error data, we evaluated basic system dependability characteristics such as error and failure distributions and hazard rates for both individual machines and for the VAX cluster. We also developed performability models with reward characterization to analyze the impact of errors and failures on the system as a whole.

The results show that more than 46% of all failures were due to errors in shared resources, despite the fact that these errors have a recovery probability greater than 0.99. This result indicates that shared resources (network, disks, and tapes) constitute a major reliability bottleneck for the VAX cluster due to their sheer number of errors. The hazard rate calculations show that not only errors, but also failures occur in bursts. Approximately 40% of all failures occur in bursts and involve multiple machines. This result indicates that correlated failures are significant. Analysis of rewards shows that software errors have the lowest reward (0.05 vs. 0.74 for disk errors), *i.e.*, most software errors lead to system failures. The expected reward rate (reliability measure) of the VAX cluster drops to 0.5 in 18 hours for the 7-out-of-7 model and in 80 days for the 3-out-of-7 model. The VAX cluster system availability is evaluated to be 0.993 for 250 days' operation.

By our results, correlated failures and software errors are two prominent dependability issues for the VAX cluster. We are investigating these issues by performing error/failure correlation analyses and a detailed software error analysis. The preliminary results of correlation analyses show that errors are highly correlated across machines (most correlation coefficients > 0.6). Although the failure correlation coefficient is not high (average = 0.15), it significantly affects system availability. The widely used analytical availability model that does not consider correlated failures is found to underestimate system unavailability by an order of magnitude for the (1-out-of-2) VAX cluster system.

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WORK UNIT NUMBER 11

TITLE: Efficient Computation Techniques

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SCIENTIFIC OBJECTIVE:

The analysis and design of efficient computation techniques has been for several years one of the most vigorous areas of research in information processing. Its impact has been not only on the availability of better computational methods for a number of significant applications, but also on the awareness both in the computing community and in the users' community of the crucial importance of algorithmic design. By investigating both upper and lower bounds to the resource requirements of specific applications and by developing effective methods for designing parallel VLSI algorithms, this discipline effectively develops a methodology aiming at a quantitative formulation of the inherent difficulty of problems in technology-driven computational systems.

The involvement of our research group with this topic is well established and dates back to the early seventies. Our record over this period shows that our focus (as well as that of our peer community) has been adjusting dynamically, as evolutions in technologies continuously modify the general research horizon and the perception of relevance. The most significant development of this type has been the advent of Very-Large-Scale-Integration (VLSI), which has profoundly influenced essentially every facet of our current research interests. The advent of VLSI is important in two major respects: one is the present possibility to realize massively parallel computers; the other is the introduction of criteria of complexity (the VLSI "model") that takes into account the design rules dictated by current technology.

Thus, parallel computation is, again, the dominant theme of the research outlined in this proposal, with particular emphasis on applications that are significant for JSEP. This research interest, of course, will not entirely replace our traditional interest for conventional serial computation, with which it constructively and productively interacts. In fact, the study of serial algorithms benefits the development of parallel algorithms, either because of direct parallelizability or because of the obtained insights on the structure of specific problems.

SUMMARY OF RESEARCH:

We have studied the systematic mapping of problems on SIMD array processors and multiprocessors. The general problem of optimally mapping any asynchronous computation on a multicomputer system is NP-hard. We have studied a restricted class of asynchronous computations that are represented by the learning of weights in a multilayer feed-forward neural network [7,8]. The objective is to minimize the completion time of parallel neural-network simulations. By noting that the computation time is predominant over the communication time in most cases, a simplified efficient algorithm with negligible error is developed and analyzed. Experimental results for mapping on an Intel iPSC/2 computer and a network of Sun computers have been carried out and are found to be very close to those predicted by analysis.

In the coming year, we plan to carry out more extensive experiments on this mapping algorithm. We will study the mapping of an asynchronous network of computations on a network of the Intel iPSC computer, the Stardent multiprocessor, and the Sun network. We will develop conditions that will allow isomorphic mappings to be found efficiently. We will further extend our results so they can be applied to nonuniform recurrence equations.

We have also investigated a number of parallel algorithms to be executed on fixed interconnections. Specifically we have demonstrated the existence and feasibility of a universal expression evaluator, a module that augments the power of ALUs and may potentially replace them. We have also investigated the parallel execution on the cube-connected-cycles of an important primitive in computational geometry. Other investigations in computational geometry have led to algorithms that are both interesting in their own right and are first steps towards parallel implementations. Finally, we have undertaken the traffic analysis of a complex optical interconnection system, realized as a Butterfly network. We have developed a novel modelling and obtained novel results on the statistical behavior of such networks, soon to be presented in a technical report.

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WORK UNIT NUMBER 12

TITLE: Computer-Aided Design of Very High-Speed Integrated Circuits

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SCIENTIFIC OBJECTIVE:

Computer-aided design of integrated circuits has been the subject of many research activities for a number of years, both in universities and industry, and many CAD tools have been developed to aid in the design and analysis of integrated circuits and systems. However, there are still many basic issues that must be resolved as the processing technologies evolve and device feature sizes shrink. To manage the increasing complexity of VLSI designs, hierarchical techniques are employed. At each level in the hierarchy, the design is often guided by an attempt to minimize a certain cost function satisfying a set of constraints. The need for developing efficient CAD tools to produce optimum designs is becoming more apparent, particularly for high-performance custom or semi-custom chips. Automatic synthesis techniques that produce optimized designs from higher level specifications are needed. For example, synthesis techniques that minimize the number of devices needed in implementing functional specifications would be desirable. At the same time, the design needs to be easily testable and reliable. The performance of the design in terms of area and speed needs to be optimized. Different design styles offer different trade-offs between area and speed. The effect of interconnect parasitics on speed is becoming more important as feature sizes shrink. Thus, designs that use two or more metal layers of interconnects are becoming viable techniques to improve speed.

Other important issues that must be addressed include chip reliability, both short and long term, and chip yield. This requires the development of statistical analysis techniques. Statistical analysis is essential in order to insure that fabricated integrated circuits would meet performance specifications with a reasonable yield. The random nature of process variations makes it difficult to predict the distribution of performance statistics and hence the chip yield, unless the design is carried out by using the so-called worst-case analysis. In practice, the worst-case analysis is often used mainly because it guarantees that almost all functional devices would meet parametric specifications. However, the worst-case analysis imposes too much of a burden on the process development and is often overly pessimistic. The state-of-the-art design should take advantage of new technologies and hence requires in-depth statistical analysis to make the design robust to process variations as much as possible. This does not mean that statistical design methods alone can solve the yield problem. Rather, the statistical design approach treats the variations in circuit performances as noise and attempts to find an optimal design that provides a good yield.

The objective of this proposed research is to develop analysis and design automation techniques for reliable high-speed integrated circuit designs. This includes the automatic synthesis of testable circuits with a reduced number of devices, automatic generation of layout using two metal interconnects, and the development of mathematical methods and algorithms for optimizing the design. The work will also include the development of rigorous and systematic statistical design techniques that are computationally efficient and hence applicable to the design practice of VLSI circuits or exploratory development of high-performance integrated circuits.

SUMMARY OF RESEARCH:

In the area of automatic circuit synthesis, we have developed an approach that automatically generates a transistor-circuit netlist from a high-level specification, such as Boolean functions or truth tables. The approach uses switching network logic models and is capable of synthesizing circuits with a minimum number of transistors. The method has been developed and implemented to design both combinational and sequential circuits [2,21]. A design system has been developed that couples the synthesis approach to a layout system based on the Metal-Metal Matrix (M^3) design style [3-5,9,10, 21]. We are thus able to automatically generate circuit layout from functional specifications.

In the area of design verification, we have explored the parallel implementation of relaxation algorithms for circuit simulation based on the Gauss-Jacobi and the Gauss-Seidel methods. Simplified speedup estimates are used in a presimulation selection procedure that selects the fastest of the parallel relaxation algorithms prior to performing the simulation of a given circuit on a given number of processors. The parallel relaxation algorithms have been implemented in programs that run on an 8-processor Alliant FX/8 multiprocessor computer [34,38]. We have also studied the convergence properties of the Gauss-Seidel and Gauss-Jacobi algorithms and proved theorems that help in constructing circuit partitioning algorithms that ensure the convergence of the relaxation process [28].

We have also developed and implemented a dynamic partitioning method based on piecewise-linear device characteristics that produced computational speedups of two orders of magnitude compared to standard circuit simulation. Simulation using the dynamic partitioning method on the Alliant FX/8 multiprocessor computer indicates efficient use of the processors and corresponding improvement in speed [1]. We have also developed and implemented parallel circuit simulation algorithms based on the direct method and on nested partitioning techniques to be used in the simulation of circuits containing detailed complex models [11]. Computational speedups of up to 7 were obtained using an Alliant FX/8 multiprocessor computer with eight processors. We have also implemented the approach as a multilevel parallel solver for block tridiagonal and banded systems on a hypercube [12].

For very large digital circuits, however, detailed waveform simulation, even when parallel processing is used, may not be cost effective and, perhaps, not necessary for verifying the operation of a large portion of the design. In this regard, we have developed a nonlinear macromodeling approach where a subcircuit structure is automatically reduced to a parameterized inverter circuit. The macromodeling approach splits the subcircuit into transistor gate information and loading information. In a given design many subcircuits have identical gate configurations, but each instance of a gate has a unique RC loading condition. During simulation the gate and loading information are combined and used to calculate output node voltage changes. All necessary information needed for voltage calculations is precomputed and stored in tables. Using the proposed macromodeling and the delay method greatly reduces simulation time [31,32,36,39]. We have also developed fast algorithms for logic simulation [37], and for fault simulation [30,40].

We have also developed novel probabilistic simulation techniques for reliability analysis of VLSI circuits for electromigration estimation [29,33,35] and MOS transistor modeling for hot-carrier effects [25]. Reliability is becoming increasingly important, especially with the dramatic increase in the number of devices on a chip, with the corresponding decrease in feature sizes; and the increase in operating frequency and speed.

To manage the increasing design complexity of VLSI integration, it is critical to improve the computer-aided design (CAD) tool capabilities in both computation time and accuracy. In the conventional approach, improving both computational efficiency and accuracy has been contradictory and deemed infeasible. Recently much research and development have been carried out to shorten computation time required for circuit verification by using simplified models for transistors, logic gates, and macrocells. Switch-level and fast timing simulators have been introduced for practical timing verification with some sacrifice in accuracy. Since state-of-the-art VLSI circuits often include both analog and digital circuits, electrical performance verification requires so-called "mixed-mode simulation" that combines the advantages of both switch-level simulation for digital circuits and more accurate transient simulation for analog circuits. A major problem in mixed-mode simulation has been in the interface of crude switch-level waveforms and more detailed analog waveforms. It is indeed a serious bottleneck since the nature of handling digital circuits (switch-level simulation) has been quite different from the conventional circuit-level simulation.

We have undertaken a drastically different simulation approach to address this issue. We have assumed that I-V characteristics of MOSFETs can be modeled by a second-order polynomial as in the case of level-1 SPICE model. Although it would be inferior to using much more complex MOSFET models, such an approach can be effective for solving fast timing simulation problems and at the same time solving the interface problem.

As for the technical details of this approach, this new approach is to develop and use analytical solutions of state equations in which nonlinearity is limited to second-order polynomials. Since analytical solutions are used instead of numerical integration, a significant saving can be achieved in simulation time as long as such state equation models are valid. At the same time, the solution waveforms are practically analog and well suited for interfacing with analog circuit-level simulation. To date we have demonstrated the feasibility of this approach by comparing our results against state-of-the-art switch-level and fast timing simulation results using 50-stage inverter chains and other small benchmark circuit examples [6]. More difficult tests using much larger circuit examples remain to be done after fully developing the new simulation capability.

We have also developed a very general circuit primitive with which flattened VLSI circuits can be decomposed into analytically solvable circuit modules. For the representative primitives, a total of 13 separate analytical solutions have been found for different operating conditions and coded into the simulation program. The simulation of individual circuit primitives already has demonstrated unique capabilities not available in the previous fast timing or switch-level simulators. For instance, the new simulator can accurately simulate CMOS XNOR gates much faster than SPICE, while other simulators fail to simulate such a gate.

One of the remaining difficult problems is to handle DC-connected blocks of multiple primitives efficiently. We are investigating mapping techniques that can map blocks into an equivalent primitive for which fast analytical solutions can be found. A simpler mapping technique has been commonly practiced in previous approaches and its usage is not unique to the proposed approach [36]. A solution of this problem would enable us to compare larger benchmark circuits to further demonstrate the feasibility of this new approach. It would also be of significant technical interest to perform mixed-mode simulation of mixed analog digital circuits using the proposed approach as the simulation engine of digital circuits.

In designing an integrated circuit, it is important to fix the sizes of transistors in the circuit so as to minimize the overall delay, while ensuring that its area is within reasonable limits. For the efficient design of a CMOS digital circuit, there are two important criteria that the circuit designer attempts to satisfy, namely,

(a) To minimize the worst-case delay of the circuit. This enables the circuit to be operated at a faster speed and from a more holistic viewpoint, allows a faster throughput for the system.

(b) To minimize the area of the circuit. A reduction in area has numerous advantages, the most significant of which are higher packing density and reduced power consumption.

To satisfy the first criterion, the sizes of certain transistors in the circuit need to be substantially increased beyond the minimum size allowed by the fabrication technology. This may, however, make the area intolerably large, for which the penalty of reduced density must be paid. Additionally, an increase in area implies an increase in the circuit capacitance, which could possibly, in turn, retard the speed of the circuit. Hence the delay and area are closely interlinked, and one seeks to find a set of transistor sizes that gives a satisfactory trade-off between them.

During the past year, under JSEP sponsorship, we have developed iDEAS: a delay estimator and optimal transistor sizing tool for combinational CMOS circuits [19]. The focus of this work has been on developing an optimization algorithm that takes advantage of certain features of this problem to give a fast and accurate solution of the problem. Additionally, a relatively sophisticated delay estimator is employed, which recognizes the fact that rise and fall delays may be different and accounts for this while computing the overall delay through the circuit.

The algorithm in iDEAS is presently applicable to sizing clocked sequential circuits, where each stage of the clocked circuit is combinational. In such circuits, the overall speed of operation is dictated by the stage that has the maximum delay. Thus, in order to allow the circuit to be operated under a given clock frequency, the designer's goal would be to ensure that the delay of each stage is less than the clock period. The algorithm could then be applied successively to each stage to generate a set of transistor sizes that ensure that the circuit operates at the fastest possible clock frequency, without taking up exorbitant amounts of area.

There have been several approaches suggested in the past for solving the transistor sizing problem [49-51]. The approach in iDEAS is to formulate the delay function as a posynomial in the set of transistor sizes and to recognize that such a function is unimodal, which implies that any local minimum is also a global minimum. This precludes the need for a hill-climbing optimizer and permits a simple descent type of algorithm to be used successfully.

The algorithm in iDEAS begins by initially choosing all transistors to be of the minimum size permitted by process technology. The sizes are taken to be the widths of the transistors; their lengths are kept constant. The transistor sizing problem is tackled by finding the critical path through the circuit and reducing the delay by changing the sizes of transistors along this path. The optimizer formulates a delay function for the path and performs a Gauss-Seidel type of iteration to give a new set of sizes for these transistors. This process is repeated until the area-delay product is minimized. It must be emphasized that at each iteration of the above algorithm the sizes are increased only where necessary, i.e., sizes of transistors not appearing on the critical path remain unchanged.

iDEAS uses a gate-delay model that is the same as the one in TILOS [49,50] and is based on the notion of the Elmore time-constant [56]. However, the optimization method used to change the transistor sizes differs from that used by TILOS; it allows uninhibited changes about the present set of sizes and permits both increments and decrements from the current value. Moreover, unlike TILOS, where the size of only the transistor with the largest sensitivity is increased in every iteration, iDEAS allows changes in the size of all transistors along the critical path of the circuit.

Several combinational CMOS circuits have been sized by using iDEAS. In each case it was found that iDEAS provided a significant improvement over the initial unsized circuit in terms of the area-delay product. The unsized circuit referred to here is a circuit with all initial transistor sizes set to 3λ, where $\lambda = 1.5\ \mu m$ denotes the minimum feature size. For example, on a chain of five CMOS inverters, the area of the unsized circuit was $1300\ \mu m^2$ with a delay of 29 ns. After sizing the transistors by iDEAS, one obtains an area of $2322\ \mu m^2$ and a delay of 8 ns thus reducing the initial area-delay product by approximately 50%. On a 4-bit combinational full adder circuit, the unsized circuit had an area of $30420\ \mu m^2$ and a delay of 95 ns, while the circuit sized by iDEAS had an area of $44222\ \mu m^2$ with a delay of only 43 ns.

It has been observed that the total CPU time required by iDEAS increases less than linearly with the number of transistors in the circuit. The delay values estimated by iDEAS were compared with those obtained from SPICE2 [57] and were found to be within 20% of the SPICE values.

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WORK UNIT NUMBER 13

TITLE: Adaptive Systems for Identification, Filtering and Control

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SCIENTIFIC OBJECTIVE:

Our major goal is the fundamental understanding of how to design high-performance and robust adaptive systems for use in control, filtering, estimation, and identification.

Adaptive systems are comprised of algorithms that utilize information acquired on-line to modify the system. The goals of this modification are several. First, the resulting system should be stable. Second, by fine tuning the controller on-line, using the most recent data to model the system, the performance of the system can be optimized.

The basic component of all adaptive algorithms consists of a parameter estimator, the most common one being based on least-squares. The fundamental behavior of such least-squares algorithms, in particular their stability and convergence performance, is a basic and most important issue about which little is known. Some very recent results obtained by us exhibit the promise of providing a broadly applicable analysis of least-squares estimation algorithms in a variety of environments.

A second issue of interest is the *self-tuning* properties of adaptive systems; i.e., will adaptive systems automatically tune themselves to optimal controllers? We intend to investigate the self-tuning property of the minimum variance regulator as well as its generalizations and predictive control algorithms.

A third issue of importance is the *robustness* of adaptive controllers. Since adaptive controllers and estimators are highly nonlinear stochastic systems, their stability can be adversely affected by unmodeled dynamics and disturbances. A sound understanding of such instability phenomena, as well as safety fixes, is essential. In this regard, we will investigate a promising novel approach to robust adaptive control. Our approach essentially attempts to a synthesis of H^{∞}-optimal control with adaptive feedback strategies. This scheme is particularly appropriate for treating the effects of unmodeled dynamics and exogenous disturbances.

A key reason for using "adaptation" is to automatically tune the behavior to match slowly drifting, time-varying systems. We will examine the stability and performance issues involved in such tracking problems.

Lastly, adaptive control is beginning to make the crucial transition from applicability to linear systems to applicability to fundamentally nonlinear systems. Though such nonlinear environments introduce their own set of design issues, they also allow quicker parameter convergence due to the "excitation" introduced by nonlinear elements. Our goal will be to develop an applicable theory of nonlinear adaptive control.

SUMMARY OF RESEARCH

In [4,11,13] we have obtained a "broad spectrum" theory of stochastic adaptive control that simultaneously addresses a whole class of adaptive systems based on the recursive least squares parameter estimator, which is most often used in practice. For systems with additive Gaussian white noise, basing ourselves on an extension of the Kalman filter [2], we have proved that the recursive least squares parameter estimates coverage. By further analyzing the "normal" equations of least squares we have shown that reasonable certainty equivalent adaptive control will be stable—thus providing a result of broad applicability. Additionally, we also establish a core set of four results that provides precise results regarding the limiting adaptive controller. As an example, for the first time ever, we have proved the convergence of the well-known self-tuning regulator for systems with additive white Gaussian noise—an open result for more than 15 years.

In [13] we have established the stability of output error identification and adaptive infinite impulse response filtering for systems in the presence of colored noise.

In [12,14] we have established the stability of a variety of well-known priority scheduling schemes for distributed systems. Motivated especially by the problem of scheduling a large semiconductor manufacturing facility, we have analyzed the First Buffer First Serve (FBFS), Last Buffer First Serve (LBFS), Earliest Due Date (EDD), and a new Least Slack (LS) distributed scheduling policy that performs very well. All these results were outside the scope of known results in queueing networks.

Another area of application for adaptive techniques is the control of nonlinear systems. Common to all of the existing literature on this subject is the restrictive assumption of full-state measurement. In a very recent paper [29], however, we obtained the first ever results on adaptive control of nonlinear systems using only output measurements. We hope that this ongoing research will bring adaptive nonlinear control research more in line with the practical needs and considerations of control engineers.

We have developed an H_∞ optimal control theory that explicitly accounts for transient response behavior resulting from uncertain initial conditions [16]. This is done by introducing a cost functional that represents the 'worst-case' regulation over the uncertainty in the initial conditions and the exogenous disturbances. We have treated both the finite and the infinite horizon versions of this problem formulation and have provided explicit state-space formulae for the solution.

We have also devoted considerable attention to the problems of robustness in adaptive feedback systems. In particular, we have developed a promising adaptive feedback architecture where optimal performance is obtained by adapting between several robust (H_∞-optimal) controllers. Using this architecture we have been able to exhibit a tuning algorithm that allows us to asymptotically recover optimal performance in the context of disturbance rejection. We are currently evaluating the effectiveness of this adaptive strategy to a half-car active suspension control problem.

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WORK UNIT NUMBER 14

TITLE: Decentralized, Distributed, and Robust Systems

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SCIENTIFIC OBJECTIVE:

Advances in communications and computer engineering, together with the recent developments in solid state sensors technology, provide the opportunity for *decentralized* and *distributed* control of large dynamic systems, using distributed information processing. Typical large dynamic control systems problems include flexible aircraft control, ship steering, vibration and control of large flexible space structures, and remote control and navigation of all-terrain vehicles. Distributed control of such systems exploits the dynamic response characteristics of materials and solid state sensors, processors, and actuators for combined passive and active control configurations. Such systems utilize locally generated process measurements together with local control inputs to obtain satisfactory global dynamic response characteristics in the presence of system modeling uncertainties (including unmodeled dynamics) and disturbance inputs.

Decentralization means that each local controller uses only part of the available information, and the **distributed** nature arises because the overall task of controlling the large dynamic system is broken up into individual subtasks that are distributed among the local controllers. The general goal of our research is to obtain a fundamental understanding of the structural aspects of decentralized and distributed control and to develop corresponding methodologies for optimum distribution of tasks among available individual controllers, yielding high nominal performance, good disturbance rejection, and robustness in the presence of modeling uncertainties. For the latter, special attention will be given to systematic design methodologies for low-order dynamic controllers, and controllers with structural constraints, in order to meet engineering specifications such as the sampling rate, computation time, and active/passive decomposition based on response characteristics of employed materials.

The problem of optimum distribution of control tasks among individual local controllers also involves, at a higher level, the optimum design of information and data transmission links for control and decision-making purposes that will support the requisite (possibly asynchronous) communication among the control stations. Such designs, under physical implementation constraints, pose challenging deterministic and stochastic optimal control problems whose solutions require the development of new methodologies and novel analytical and numerical techniques. Pursuing this will be another objective of our research.

SUMMARY OF RESEARCH:

During this period, one aspect of our research activities in robust systems has been concentrated on designing minimax controllers for systems subject to unknown norm-bounded disturbances. Using a game theoretic approach, we have been able to solve completely the discrete-time disturbance rejection problem for linear time-varying plants when perfect state measurements or their delayed versions are available to the controller—obtaining the best achievable performance bound and a characterization of the linear controller that achieves it [6,8,9]. This linear controller turns out to be in saddle-point equilibrium with a correlated random disturbance, which shows that, interpreted as a dynamic game, the problem does not admit a pure-strategy saddle point. One of our other findings in this framework is that if the norm bound on the disturbance is known (and fixed), there exist nonlinear controllers that lead to better performances for the system (than the best linear controller) should the disturbance occur outside the support set of the worst-case distribution [5]. These results were first obtained under l^2 norms and then extended to l^1 norms [7]. Furthermore, the initial state of the system has been taken to be either a completely unknown quantity (thus treated as a disturbance) or a known (possibly nonzero) quantity [11].

We have also studied the disturbance rejection problem for continuous-time systems and have developed a general methodology for obtaining the so-called H^∞ controller under different measurement schemes, using the feedback saddle-point solution of a particular differential game [10]. The information structures considered include the perfect state, delayed state, and sampled state measurement schemes. In each case the minimax disturbance attenuation bound has been obtained in terms of conjugate points of some Riccati differential equations.

In the design area, we have concentrated on methodologies to meet simultaneously several diverse requirements including transient performance, disturbance rejection, robustness, and reliability, using:

- low-order controllers to satisfy the basic performance, disturbance-rejection, and robustness requirements;
- full-order output-feedback controllers, of the same order as the plant, to improve the reliability of the system by being capable of withstanding outages of sensors and actuators; and
- output-feedback controllers for decentralized systems to meet requirements associated with transient performance, disturbance rejection, and reliability.

The design methodologies we have developed are based on:

- projective controls, which provide a parametrized family of low-order controllers that guarantee certain performance specifications are met and possess free parameters to be used to meet additional requirements [12,13,14];
- the Frobenius-Hankel (FH) norm as a computationally attractive measure of optimality to meet disturbance rejection and robustness requirements with low-order projective controllers [12,13,14,15,16];
- the algebraic Riccati equation as a means of characterizing H_∞-norm-bounding controllers, including:
  — state-feedback controllers to provide the reference solution for the projective controllers and
  —full-order output-feedback controllers that meet robustness and reliability requirements, or solve the decentralized control problem.

Our research has encompassed many issues not treated previously. These include the development of better bounds on the H_∞-norm for established ARE-based designs [17] and the study of the properties of the convex Riccati operator and the associated algebraic Riccati inequality $R(X) \leq 0$ [18]. These properties were fundamental in rederiving in simple terms the state-feedback and output-feedback H_∞-norm-bounding controllers and extending the procedure to achieve robust stabilization with an H_∞-norm bound in the presence of structured uncertainty [19]. Also, a new parametrization of all state-feedback and output-feedback controls that guarantee a specified H_∞-norm bound [18] has been obtained.

In [17,21,22] the approach was extended to the design of controllers for decentralized systems. It was shown that a controller of the same order as the system can be developed for each control channel by constructing for each channel an observer in which the controls associated with other channels are replaced by the estimates of these controls, as they are defined by the state-feedback solution to the H_∞-norm-bounding problem, and the disturbance is replaced by the worst disturbance as described by the same state-feedback solution. The observer gains for the controllers are determined by the positive definite solution of a large-dimensional ($n \times r$, where r is the number of control channels) Riccati-like algebraic equation.

The developed design methodology was extended to the problem of design of reliable control systems [20,23]. This includes the design of strongly stable closed-loop system and controllers robust to the loss of a selected subset of measurements, or control inputs.

Contributions to H_∞-norm optimal and H_∞-norm-bounding controls for discrete-time systems include the establishment of a lower bound for the achievable H_∞-norm that complements the known upper bound, a study of the properties of the discrete convex Riccati operator, and the development of the design equations for the output-feedback H_∞-norm-bounding controllers for discrete systems by utilizing a transformation of the DARE to a Generalized (continuous) algebraic Riccati equation (GARE) [24].

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WORK UNIT NUMBER 15

TITLE: Sensor-Array Imaging of Dynamic Scenes

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SCIENTIFIC OBJECTIVE:

In some sensor-array imaging systems, many spatially disparate sensors are used to sample the input signal; in others, a single sensor is moved from one spatial location to another. Important types of sensor arrays include synthetic aperture radar (SAR), X-ray computer tomography (CT), and scanning laser range-fingers. In many applications, during the total data collection period, the scene being imaged changes with time due to motion so that the sensors do not "see" the same scene from every spatial or angular vantage point. For example, this occurs in SAR imaging of moving vehicles or in CT imaging of the beating heart.

The objective of our research program is to study the basic issues in using sensor arrays to image dynamic scenes, including the detection, estimation, and correction of motion, and the optimal design of image acquisition systems. In our study, we plan to examine both the single-frame and the multiple-frame cases. We are mainly interested, however, in the case where the amount of object motion or scene change is significant during the time interval used to collect one image frame, not in the case where the effects of the object motion within a single frame can be neglected.

In the case of small motion during the data collection interval, the effect of the motion is to blur the desired image. For this case, we hope to quantify and characterize the image degradation resulting from scene motion and to develop algorithms to detect the moving parts of the scene and correct for the blurring. In the case of large motion, our aim is to detect and track moving targets and to estimate their motion parameters. In both the small-motion and the large-motion cases, we are also interested in designing optimal acquisition schemes to facilitate the tasks of motion detection, estimation, and correction.

SUMMARY OF RESEARCH:

During the past year, our research has focused on four facets of sensor array imaging of moving scenes: 3-D motion estimation, tomographic imaging of time-varying distributions, interpolation from nonuniformly spaced data, and waveform design for range-Doppler radar. In the area of 3-D motion estimation, we are investigating techniques for estimating the 3-D motion parameter of rigid objects from data received by radar or sonar sensor arrays. Two approaches are being pursued:

(i) 2-D images of the objects are first constructed at discrete time instants, then 3-D rotation and translation of the objects between two consecutive time instants are estimated using feature correspondences.

(ii) 3-D motion parameters of the objects are directly estimated from the signals received by the sensor array.

During the period covered by this report, our work was concentrated on approach (i). Specifically, a new extrapolation algorithm was developed in connection with the 2-D image construction stage [7]. For the stage of 3-D motion estimation from feature correspondences, we developed a robust method of extracting and matching line features over several images [6] and several linear and nonlinear algorithms for determining 3-D rotation and translation from point and line correspondences [3,4]. We are currently turning our attention to approach (ii): estimating the 3-D motion parameters directly from received sensor array signals.

During recent months, we have focused an effort on tomographic imaging of time-varying distributions. In [5] we addressed the case in which the temporal variation during acquisition of the data is high, precluding Nyquist rate sampling, and a-periodic, precluding reduction to the time-invariant case by synchronous acquisition. The impact of the order of acquisition of different views on the image-domain reconstruction error was determined for band-limited temporal variation. Based on this analysis, a novel technique for lowering the sampling rate requirement while preserving image quality was proposed and investigated. This technique involves an unconventional order of sampling the projections, which is designed to minimize the energy of the reconstruction error of a representative test image. In computer simulations of some images, a a seven-fold decrease in the error energy was observed using the optimized sampling scheme, compared to conventional sampling. The results indicate the potential for efficient acquisition and tomographic reconstruction of time-varying data. Application of these techniques are foreseen in SAR imaging, X-ray computer tomography, and magnetic resonance imaging. An invention disclosure on the technique was filed with the university of Illinois, which is evaluating it for possible patent application.

Our work on interpolation from nonuniformly spaced data is motivated by the fact that many sensor-array systems provide data on a non-Cartesian grid. In SAR and tomography, for example, the data may be on a polar grid, whereas for radio astronomy, the grid may be highly irregular. Image reconstruction in these systems frequently involves a complicated interpolation. In [1] we used a linear time-varying systems framework to model interpolation from nonuniformly spaced data. This framework provides a frequency-domain description of the interpolation process and permits the design of 1-D interpolators through the use of 2-D digital filter design techniques. A 2-D frequency sampling approach was explored as a means of producing a better approximation of an ideal interpolator.

Range-Doppler radar has long been used to estimate the range and velocity of a moving target. Furthermore, a 2-D range-Doppler image can be produced by utilizing a bank of matched filters. The performance of such systems is determined by the ambiguity function of the transmitted waveform, which characterizes the range and Doppler resolution trade-off. In some preliminary work described in [2], we derived an exact expression for the continuous ambiguity function of a time-limited waveform in terms of the discrete ambiguity function of the same waveform. We then solved the problem of least-squares synthesis of discrete ambiguity functions for time-limited sequences. The dual problem of synthesizing ambiguity functions using bandlimited waveforms can be solved in a similar way, as can the least-squares design of Wigner distributions. This work is continuing and it has resulted in some important publications that will be described during our next reporting period.

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WORK UNIT NUMBER 16

TITLE: Topics in Survivable Communication Networks

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SCIENTIFIC OBJECTIVES:

The general objective of this unit is to improve the state of the art in survivable communication networks by investigating some critical issues in communication network design and performance. A better understanding of the fundamental trade-offs between communication efficiency and survivability will be obtained, and improved modulation and coding schemes, receiver processing techniques, and network protocols will be developed for use in communication networks that will be subjected to jamming, fading, and loss of resources.

Improved adaptive coding techniques and adaptive protocols for meteor-burst communication will be developed, and the role of meteor-burst communication links in mixed-media communication networks will be investigated. New methods for modulation, transmission, and coding will be obtained for use in frequency-hop communication over HF and other channels with fading, partial-band jamming, and various forms of radio-frequency interference. Synchronization procedures for spread-spectrum signals will be investigated, with particular emphasis on channels with multiple-access interference and fading. Finally, a better understanding of network-directed electronic countermeasures (ECM) will be sought, particularly those concerned with thwarting traffic analyses and operating under emission control.

STATE OF THE ART:

Survivability is perhaps the most important requirement for modern military communication systems and networks, yet much remains to be done to provide it for the communication environments that will be encountered in the future. The problem is complicated by the large number and wide variety of potential threats present in a battlefield environment, including aggressive electronic countermeasures that range from jamming to sophisticated attacks against network protocols. The RF environment for modern military communications is corrupted by a large number of non-Gaussian sources of interference including other-user interference and intelligent jammers. The potential disruption of communication by such interference, along with the possible loss of some network resources, can lead to a loss of network connectivity, particularly in networks with high mobility or those with only a small number of communication platforms in a given region. The communication and synchronization capabilities that are needed to reconfigure a network under stress are difficult to ensure. While spread-spectrum signaling, in conjunction with diversity transmission and error-control coding, has been quite successful in providing a certain level of anti-jam (AJ) and low-probability-of-intercept (LPI) capability, there remains a great need for improved synchronization methods for acquisition in the presence of interference, adaptive signaling and coding methods for meteor-burst channels and other time-varying channels employed by military systems and networks, and novel network-based ECCM techniques.

PROGRESS:

Meteor-Burst Communications

We have completed an investigation of the application of incremental redundancy transmission to meteor-burst communication systems with Reed-Solomon codes. In this type of transmission, also referred to as type-II hybrid automatic repeat request (ARQ), the source, upon receipt of a negative acknowledgment for a given data block, sends additional parity check symbols associated with the data block. These symbols, along with those received in the first transmission for this block, are used in a decoding attempt at the destination. In [18] we compare the performance of type-II hybrid ARQ with that of fixed-rate type-I hybrid ARQ. We show that, in terms of the throughput per meteor trail, the throughput is larger for type-II hybrid ARQ than for either fixed-rate type-I hybrid ARQ or ARQ without forward error correction.

In [19], we introduce a form of ARQ, referred to as variable rate type-I hybrid ARQ, in which the code rate varies in response to the fluctuations in the power received from the meteor trail. In one approach, the source periodically obtains estimates of the signal power at the destination, and the source uses these estimates to select the rate of the code. In an alternative approach, the code rate is determined completely by the history of decoding successes and failures during previous transmissions. This latter approach is much easier to implement in a practical meteor-burst communication system. We show that the throughput is larger for either of these approaches than for fixed-rate type-I hybrid ARQ or ARQ without forward error correction.

Acquisition of a Direct-Sequence Spread-Spectrum Signal

We have studied the use of the sequential probability ratio test (SPRT) for the coherent acquisition of a direct-sequence spread-spectrum signal that uses a maximal-length shift register sequence (pseudonoise or PN sequence) [1]. Consider a correlator that multiplies the incoming sequence with the local reference sequence and integrates the result. The integrator is sampled once every chip and then dumped. When the incoming sequence is in phase with the local reference sequence, the correlator output is a sequence of independent identically distributed unit variance Gaussian random variables whose common mean μ is a measure of the signal-to-noise ratio. On the other hand, when the incoming sequence is not in phase with the local reference sequence, the correlator output is a sequence of unit variance independent Gaussian random variables whose means have value $\pm\mu$. The sequence of means is itself just some unknown phase shift of the PN sequence. The fact that this phase shift is unknown leads to difficulties in analysis, and previous studies of acquisition methods have modeled the out-of-phase output sequence simply as a sequence of zero-mean Gaussian random variables. In our study, we have replaced this zero-mean model with a random sequence model. Here, the sequence of means is itself a sequence of independent identically distributed random variables taking on values $\pm\mu$ with equal probability. Since the actual sequence of means is a *pseudorandom* sequence, we feel that a *random* sequence is a better and more accurate model for the mean sequence than a zero sequence.

In practice, the integrator in the correlator is not sampled and dumped after each chip. Instead, the correlation is performed over several chips. Such a correlator computes the optimum statistic for an SPRT if the out-of-phase sequence happens to be a zero-mean sequence. However, the out-of-phase sequence is not a zero-mean sequence. We have determined the optimum statistic for the SPRT based on the random sequence model and have devised new methods for comparing the performance of an acquisition system based on this optimum statistic with the performance of a standard acquisition system based on correlating over several chips. In each case, it is assumed that the random sequence model is valid, and the performance measures are the probabilities of error and the expected sample sizes, that is, the mean time to acceptance and the mean time to rejection of the hypothesis. We have found that the mean times to acceptance or rejection are very nearly the same for both systems. However, the standard system's probabilities of error degrade significantly as the signal-to-noise ratio increases. Details are given in [1]. We have also studied truncated SPRTs and obtained similar results.

Analysis of Transmission Scheduling Algorithms

During the past year we suggested and analyzed the performance of several algorithms for communication to a silent receiver, under JSEP support [20]. The basic scenario [21] is that several transmitters wishing to communicate to a single silent receiver simultaneously send messages using different spread spectrum codes. The receiver must schedule when to listen to the various messages. The messages may be sent multiple times, to counteract conflicts. We tested the performance of the maximum matching algorithm, which can be used to maximize the number of transmitters that are listened to at least once each.

New algorithms were proposed and tested that take into account the effect of secondary interference. Slots with fewer messages transmitted in them have a higher level of secondary interference, and that is accounted for when the slots are distributed among the messages. The load balancing algorithm developed recently under JSEP support [3,4] was applied. Another innovation was to investigate the use of incremental redundancy. In this approach, a given receiver does not simply transmit its message several times. Rather, the message is coded differently each time so that any combination of copies of the transmitted messages form part of a large Reed-Solomon codeword. This improves the error correction capability.

The major conclusion is that the various techniques tried improve the performance. Moreover, the relative impact of the methods tried was shown to depend on what most limited performance—primary interference or secondary interference. It has recently been observed that the work unexpectedly may find application in high-speed communications with large propagation delay, as might occur over a satellite link or high-rate fiber optic wide-area network, where acknowledgments are only available after a long delay.

Sequential Decoding with Adaptive Reordering of Codeword Trees

We have invented and investigated a new method of providing forward error correction, based on a new sequential procedure for decoding certain block codes, under JSEP support [22]. We call the new decoding algorithms sequential decoding with reordering (SDR) algorithms. They observe the received message at the channel output and use this information to reorder the digits in the codeword tree. The resulting tree is then searched by a sequential decoder; the goal of the reordering is to obtain a tree that is easy to search. Linear block codes are used in which each parity check involves a small number of bits (low-density parity check codes). The reordering algorithm is a greedy method that tries to insure that parity checks with the smallest incremental uncertainty are considered first.

Given a communication channel, there is a data rate, called the computational cut-off rate, such that for transmission above that rate the mean computation required per data bit is infinite for any sequential decoding procedure in which the parity checks are examined in order according to a fixed tree, as is typical for decoding of convolutional codes. Our variation of sequential decoding appears to allow computationally feasible operation at data rates above the computational cut-off rate. This interesting phenomenon is suggested by our simulations for the binary erasure channel and the binary symmetric error channel for channels with error or erasure probabilities that range from roughly 0 to about 0.25.

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WORK UNIT NUMBER 17

TITLE: Adaptive Signal Processing

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SCIENTIFIC OBJECTIVE:

The overall scientific objective of this unit is the development of techniques for the extraction and/or enhancement of time-varying (nonstationary) signals from additive noise. The characteristics of signal encountered in practice are often time-varying; for example, the ocean acoustic channel and the signals of interest there are all strongly time-varying, as are most high-speed communication channels of interest to the military. Nonstationary signal behavior often severely limits the performance of conventional signal analysis tools, such as FFT-based spectral analysis and narrow-band bandpass filtering. In time-varying situations, since the variation with time is rarely known beforehand, adaptivity is the key to effective system performance. In this research unit, we are developing adaptive approaches for processing several important classes of time-varying signals and algorithms to extract relevant information from nonstationary signals. We expect that these algorithms will have performance comparable to that of conventional techniques applied to stationary signals.

Both parametric and nonparametric approaches are bring investigated in this project. For narrow-band signals with time-varying frequencies, high-resolution parametric methods based on singular value decomposition are under study. For wide-band signals, we are investigating nonparametric methods such as time-frequency analysis, as well as high-resolution parametric methods based on slowly varying ARMA and AR models. For the tracking of these time-varying system models, adaptive FIR and IIR filtering methods will be investigated. The objectives are to develop computationally efficient adaptive time-frequency representations and new adaptation algorithms and adaptive filter structures that are computationally efficient for real-time applications, are robust, and are suitable for short wordlength VLSI circuit implementation.

SUMMARY OF RESEARCH:

During the last year our JSEP-supported research concentrated on four specific problems that are judged to be of fundamental importance in adaptive signal processing: (i) the study of time-scale separation techniques to improve convergence rates in both finite impulse response (FIR) and infinite impulse response (IIR); (ii) new adaptive algorithms and digital filter architectures for two-dimensional adaptive filters with improved convergence rates and reduced computational complexity; (iii) computationally efficient signal-dependent time-frequency representations; and (iv) detection and tracking of superimposed narrowband signals. Brief descriptions of the four areas follow.

(i) Time Scale Separation Techniques for Adaptive Filtering

In many adaptive filtering applications the bandwidth of the data being processed is constrained by system economics or by the limiting effects of intersymbol interference. Often this bandwidth is far less than the processing rate permitted by application of VLSI digital signal processing chips. Many processor cycles are consequently not effectively used. In such circumstances it may be possible to increase the rate of convergence by exploiting these previously wasted processor capabilities.

The notion common to many attempts to harness this unused processor ability is that the data are filtered at a rate, referred to as the processing rate, higher than the rate of incoming data, referred to as the data rate. This implicitly separates the time scale of the data from the time scale of the adaptation. The increased processing rate results in an apparent increase in convergence rate with respect to the data rate.

The notion of time scale separation is applied in many common communication systems. The fractionally spaced equalizer [43] is one example. Here the equalizer operates with a sampling interval of τ' which is less than the sampling interval of the arriving data, τ. As suggested in [44], the equalizer may be adapted at this higher rate.

The Data Reusing LMS algorithm (DR LMS) is one attempt to efficiently employ the full potential of a modern signal processing device [45]. By iterating the update relations of the LMS algorithm L times between arriving data samples, it attempts to "wring out" more information from the available data. This gives rise to two time scales: the input data rate, and the processing rate. By increasing the processing rate, the convergence rate with respect to the input data rate is increase. A trade-off is made between the arithmetic operations required per data same, and the convergence rate.

We have shown that the application of direct sequence spread spectrum (DS/SS) modulation will induce a similar change in time scales [3]. Unlike the DR LMS algorithm it does not reapply the given input data directly, but rather pseudo randomly modulates that data. This speeds the input spectrum, speeds convergence and increases the likelihood of achieving a well behaved learning characteristic by ensuring that the persistent excitation criterion is met. The time scale separation achieved by this means is particularly effective for problems in which there is a dedicated training period. Unfortunately, the DS/SS modulation cannot be easily removed after the modulated signal has passed through the adaptive filter, so this technique is difficult to apply in such applications as line enhancers and echo cancellers where the learning is done on the real information bearing signals.

Interpolation has been introduced as another means to increasing the adaptation scale and thereby increase the convergence rate. The more general study of interpolation techniques in this problem was motivated by the discovery that the DR LMS algorithm can be mathematically posed as zero order interpolation. It was demonstrated that the proper use of higher order interpolation schemes will lead to better learning rates than the more elementary DR LMS algorithm.

(ii) Filter Architectures and Adaptive Algorithms for 2-D Adaptive Digital Signal Processing

The McClellan transformation [46] is a 2-D digital filter design technique that uses a 1-D FIR digital filter prototype as the basis for obtaining a near optimal 2-D design. The impulse response (as well as the frequency response) of the 1-D prototype is mapped by the "McClellan transformation" into a 2D digital filter that inherits its frequency characteristics from the prototype. The frequency response of the 2-D FIR digital filter is controlled by the impulse response of the 1-D prototype, h(n),n=0, · · · ,N–1, and a set of five "contour" parameters A, B, C, D, and E which define the mapping. Once the contour parameters are fixed, the class of filters that can be obtained becomes "constrained", i.e., only limited types of frequency responses can be obtained by varying h(n) once A, B, C, D, and E are fixed. In particular, contour parameters have been found to produce frequency responses that are circular, elliptical, and fan symmetric. McClellan and Chan [47] later described a digital network for realizing the transformation filter which contains the h(n)'s and the mapping parameters A, B, C, D, and E as explicit multiplier coefficients in the filter structure.

An *adaptive* 2-D transformation filter, first reported in [3], is obtained by applying an LMS update algorithm to the parameters of the McClellan-Chan filter structure. When the A, B, C, D, and E's are fixed and the h(n)'s are adaptively adjusted in real-time, a constrained 2-D adaptive filter results that requires the up-date of only M+1 parameters at each iteration, where M=(2N–1)/2 and N is the length of the 1-D prototype. The classes of adaptive systems that can be obtained includes many important types of filters that are useful in real-time image processing. Computational complexity is so dramatically reduced that the implementation of such filters in real-time applications becomes an economic possibility. Also, it has been shown [48] that the convergence rate of the new structure is characterized by the 1-D prototype, and hence is much faster than a direct form 2-D LMS filter.

In our recent JSEP-supported research, three forms of the 2-D adaptive transformation filter were studied: 1) a *constrained transformation filter* which is computationally efficient but requires some *apriori* knowledge of the unknown system, an *extended transformation filter* which is not as efficient but which assumes no *apriori* knowledge of the unknown system, and a *constrained transformation filter that achieves an improved convergence rate through orthogonalization and power normalization.*

The computational complexity of the constrained adaptive filter is of order M, as compared to order M^2 for conventional direct form. The price paid for this improved performance is that the adaptive filter is "preconstrained" according to the contours which are established by fixing the mapping parameters A, B, C, D, and E. This implies that some *apriori* information about the symmetry of an unknown system must be known before this structure ca be used effectively. Both the constrained and extended filters adapt more rapidly than a conventional direct form filter. the adaptation rate falls between the extremes of the direct form 2-D on the slow side, and the rate of a 1-D filter characterized by the prototype on the fast side. Experiments show that the update direction in the (n_1,n_2)-plane does not affect the rate of convergence very much. it was found that horizontal, vertical, and 45° update directions resulted in very similar learning curves.

As in 1-D adaptive filters, the rate of convergence of 2-D adaptive filters is affected by coloring on the input noise. However, in the constrained transformation filter the rate of convergence appears to be controlled by the widest bandwidth in the 2-D frequency space, rather than by the narrowest. This means that is the input noise is wide-band along the ω_1 frequency axis and narrow-band along the ω_2 frequency axis, the constrained filter tends to adapt rapidly, as if the whole input spectrum had the widest bandwidth. In this sense the symmetry constraints imposed by the McClellan design procedure create a robust structure that selects the "best case" performance.

The extended adaptive algorithm appears to work best as a two-stage process. During the first stage the step size for the tap weights is kept smaller than that for the contour parameters so the algorithm can concentrate on identifying the contours. Once the contours are approximated, the step sizes are interchanged so that rapid convergence of the tap weights can be achieved.

When the constrained filter is driven by a white noise input signal, the transformation filters at the front end of the structure impose a coloring on the signals used to adapt the tap weights, thereby resulting in slower convergence rates than the theoretical optimum. This coloring can be removed by using an orthogonal transformation and a power normalization to white (decorrelate) the signals that drive the adaptation of the tap weights. Experiments showed that considerable improvement in convergence rate could be obtained with an orthogonal transform, although additional computation is needed to compute the transform and to normalize the power properly.

(iii) Computationally Efficient Signal-Dependent Time-Frequency Representations

We are currently developing a computationally efficient signal-dependent time-frequency representation, in which the kernel adapts to the signal to maximize auto-component concentration while suppressing cross terms. A very promising approach has been found in which the optimality criterion results in a specialized linear program which can be solved very efficiently. Preliminary experiments with synthetic data have yielded excellent results, and the computational requirements are only a few times the standard nonadaptive representations. This approach should thus be attractive for almost all applications of time-frequency analysis.

Statistical characterization of a fast method for estimating the parameters of time-varying sinusoids shows performance near the Cramer-Rao bound above a threshhold SNR [30]. Investigations have begun of extensions which promise to lower the threshhold significantly.

(iv) Detection and Tracking of Nonstationary Superimposed Narrowband Signals

Detection and estimation of multiple narrow-band components in a time-series is a difficult signal processing problem that shows up in many applications. We have been researching a parametric approach to the problem, and have developed an algorithm based on singular value decomposition (SVD) to estimate and track the parameters. The model suggested for each narrow-band component is a sinusoid with slowly varying amplitude and frequency. Thus the time-series is

$$s(n) = A_1\cos(\phi_1(n)) + A_2\cos(\phi_2(n)) + \cdots + A_r\cos(\phi_r(n)) ,$$

and the instantaneous frequency of the i^{th} component is

$$\omega_i(n) \equiv \phi_i(n) - \phi_i(n-1) , \qquad \text{for } i = 1,\ldots,r.$$

Such a model is appropriate in a multitude of signal processing systems, including interferometric direction finding for narrowly distributed sources, detection of active sonar signals, and speech processing. The slowly varying model is a more realistic and appropriate model in many systems where stationary harmonic models are used, because frequencies and amplitudes often drift with time due to changes in the source (engine speed for instance) or due to Doppler shifts when there is relative motion between source and receiver.

The conventional approach to processing slowly varying signals is to apply classical stationary techniques either to blocks of data (sufficiently small for the parameter variations over the block to be negligible) or to localized covariance estimates constructed using exponential forgetting.

The technique proposed here provides the noise reduction associated with very long averaging intervals, and yet tolerates slow drift of parameters (amplitudes and instantaneous frequencies). The algorithm is based on the rather surprising discovery that even when the frequencies and amplitudes are changing with time, a Hankel matrix constructed from the noise-free signal

$$\begin{bmatrix} s(1) & s(2) & \cdots & s(c) \\ s(2) & s(3) & \cdots & s(c+1) \\ s(3) & s(4) & \cdots & s(c+2) \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ s(N-c+1) & s(N-c) & \cdots & s(N) \end{bmatrix}$$

is close to a matrix of rank equal to twice the number of narrow-band components superimposed in the signal, as long as the change in frequencies and amplitudes over any interval of c time-instants is small, and the global change in instantaneous frequencies is moderate. The global change in amplitudes can be unbounded.

Thus, in the presence of additive noise, instead of using the SVD of multiple small matrices to suppress noise locally, global noise suppression can be achieved by using SVD-based rank reduction of a single matrix constructed from all the available data. The number of narrow-band components and the amplitude and instantaneous frequency tracks are directly estimated from the principal singular vectors of the large Hankel matrix.

The algorithm's performance has been studied by numerical experiments on computer-synthesized data. For purposes of comparison, the results of preliminary numerical studies indicate that the performance is superior to similar algorithms based on application of the corresponding stationary technique to small blocks of data and to localized covariance estimates (constructed using exponential forgetting). Analytical study of the algorithm's performance is also in progress, and preliminary analysis shows that the detection and tracking performance is independent of the global change in amplitudes, but does depend on the rate of change of both amplitudes and frequencies and on the global change in frequencies.

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WORK UNIT NUMBER 18

TITLE: Initiatives in Electronics Research

PRINCIPAL INVESTIGATOR:

W. K. Jenkins, Research Professor

SCIENTIFIC OBJECTIVE:

The objective of this unit is to provide discretionary funds to the Director for support of new initiatives on basic problems of electronic materials, devices, and systems in a timely manner and to provide early start-up funding of projects that present immediate opportunities of high scientific promise. These discretionary funds are an important feature of the JSEP program in that they support exploratory work on new topics, provide matching equipment funds in the laboratory, and support promising new faculty where appropriate.

SUMMARY OF RES ‹ RCH:

During the last three-year JSEP contract (October 1, 1986 - September 30, 1989) the entire Director's Fund of $300,000 was allocated to the new MBE facility called the EpiCenter, which is located in the east wing of the Coordinated Science Laboratory (CSL). This facility is jointly sponsored by CSL, the Materials Research Laboratory (MRL), and the newly established Microelectronics Laboratory. The EpiCenter consists of seven MBE machines interconnected by uhv ($5x10^{-11}$ torr) stainless steel transfer lines. From the same vacuum environment, it is possible to access advanced instrumentation for surface modification and sample characterization. Construction of the EpiCenter was completed during the fall of 1988, and a dedication ceremony was held in November 1988 to mark its opening. By now the facility is in regular operation and a great deal of material growth research has already been reported by researchers using this facility. The Appendix contains a reprint of an article [1] that recently appeared in *R&D Magazine* that describes the facility in considerable detail and documents the recent experiences of the researchers who are currently using the EpiCenter facilities in their research programs.

In addition to its initial investment of over $500,000 in the EpiCenter, CSL contributes approximately $40,000 annually to the EpiCenter operating fund that was budgeted during 1989 at a total of $110,000. During the first year of the current JSEP grant (October 1, 1989 - September 30, 1990) CSL will contribute approximately $25,000 of the JSEP Director's Fund toward this operating fund, with the additional $15,000 allocated from indirect cost returns. The operating budget pays the salary of a full-time research engineer who maintains the facility, and it covers various common facility expenses incurred for installation and maintenance of the equipment. The vast majority of the expenses of operating the equipment are born as direct charges to the individual research programs that make use of the EpiCenter facilities.

A portion of the JSEP Director's Fund was also used to upgrade the MOCVD equipment that is now housed in the new Microelectronics Laboratory. During the summer of 1989 the new Microelectronics Laboratory was completed and a number of JSEP senior investigators moved into the facility from their previous location in the Electrical Engineering Research Laboratory (EERL). In particular, Professor James Coleman relocated his laboratory and his MOCVD equipment to the new facility. In the process of relocation, he has put together a funding package from many different sources for a new $325,000 MOCVD system. CSL has contributed $50,000 toward the purchase of this new equipment to enhance Professor Coleman's ability to conduct device research that is important in

CSL's JSEP program. During the first year of the present JSEP grant (October 1, 1989 - September 30, 1990) $25,000 of the JSEP Director's Fund was used for this project. Since Professor Coleman has been a prime contributor to the Illinois JSEP program (having contributed to our "Most Outstanding JSEP Accomplishments" on the heterostructure hot electron diode), it is fitting that CSL participate in the upgrading of his MOCVD facilities as part of our investment in the future interests of JSEP-funded research in the device area.

At the time of the last Illinois three-year JSEP review in June of 1989, a Supplementary Unit entitled "A Study of Quantum-Well Lasers and Novel Optoelectronic Devices" proposed by Professor S. L. Chuang, received an outstanding review but could not be funded as part of the new JSEP contract due to the lack of new funds for supplementary work. Subsequently, Professors Jenkins and Chuang worked with Dr. Larry Cooper of ONR to have this project funded as a new PI grant under Dr. Cooper's initiative program in the optoelectronics sciences. In order to get this program initiated, Professor Jenkins pledged $25,000 of start-up monies from the JSEP Director's Fund during the period May 1, 1990 through April 30, 1991. This new project (Unit 20), which is now under way, is an excellent example of the leverage that can be provided by the Director's Fund in order to initiate new projects in a timely manner when unique opportunities arise.

The remainder of the first-year Director's Fund (approximately $25,000) is being used to provide partial support for several new JSEP faculty during the summer of 1990. Assistant Professors Hwu (Unit 9), Bresler (Unit 15), and Jones (Unit 17) will each receive partial summer support beyond the level normally budgeted as faculty support lines on their JSEP units so that they will be able to devote increased effort to their JSEP research. Also, Assistant Professor Sean Meyn joined CSL in the fall of 1989 (Control Systems area), and Assistant Professor Michael Orchard (Signal Processing area) will join the faculty in the fall of 1990. It is the intention of the JSEP Laboratory Director to work these two promising new faculty into the JSEP program as soon as the opportunity becomes available.

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WORK UNIT NUMBER 20
(Supplementary Unit Funded Partially by JSEP and Partially by an ONR Individual PI Grant)

TITLE: A Study of Quantum-Well Lasers and Novel Optoelectronic Devices

SENIOR INVESTIGATOR:

S. L. Chuang, Associate Professor

SCIENTIFIC PERSONNEL AND TITLES:

S. M. Lee, Research Assistant
M. I. Aksun, Research Assistant

SCIENTIFIC OBJECTIVE:

An investigation of novel semiconductor laser structures will be performed. Specifically, a nonplanar graded-index GaAs/AlGaAs quantum-well laser array will be modelled theoretically and compared with the available experimental results. Important physical mechanisms, such as the nonuniform current injection, the finite quantum-well size effects, and the optical coupled mode theory for coherent phase-locked semiconductor laser array with high power and narrow radiation beam width operation, will be investigated.

SUMMARY OF RESEARCH:

The efficiencies and output optical patterns of the nonplanar semiconductor periodic laser arrays observed experimentally by Professor J. J. Coleman's research group [3] are successfully explained using a self-consistent model, which we developed recently [2]. The nonplanar structures consist of the mesa, the bend, and the groove; each of them is formed by a graded-barrier quantum-well heterostructure. Two groups of devices of identical structures except for the different aluminum mole fractions in the cladding layers, $x=0.85$ for wafer I and $x=0.40$ for wafer II, are investigated. The theoretical results explain:

(1) The wafer I devices have better efficiencies than those of the wafer II devices because the higher aluminium mole fraction in the cladding layers of the group I devices provides a better optical confinement.

(2) The optical output intensities of wafer I devices are due mainly to the first-order mode plus some residual fundamental mode in the mesa region; there are almost no contributions from the bent and the grooved regions. The output intensities of the wafer II devices are mainly due to the fundamental and the first-order modes in the mesa region, the fundamental mode in the grooved region, as well as some residual radiation from the bent region.

These phenomena are understood via analyzing the distributions of the injected current densities, the carrier distributions, the coupling with the optical intensities, and the threshold gain variation from the mesa to the grooved regions.

optical mode pattern, and (e) the experimental data [3] in Figures 1 and 2. For the wafer I devices, the gain in the mesa is assumed to be 30% higher than that of the groove with the same carrier concentration for wafer I devices, since the spontaneous intensity in the mesa is about 30% higher when the pumping level is below threshold. We can see clearly that the theoretical optical patterns in Figures 1(d) and 2(d) agree with the experimentally observed mode patterns in Figures 1(e) and 2(e), respectively. The optical intensity in the groove is completely suppressed and the mode pattern in the mesa contains mainly the first-order mode and some residual fundamental mode intensity profiles. The gain in the mesa is assumed to be 20% higher than that of the groove with the same carrier concentration for the wafer II devices. The fundamental mode in the mesa is dominant as expected, due to its larger optical confinement as compared to that of the first-order mode. The intensities in the bend and groove are smaller than that of the mesa by a factor of five, which are more significant than those of the wafer I device. The comparable optical outputs from all regions result from the smaller gain disparities between the mesa, the groove, and the bend as well as the higher conductivity in the p-cladding layer which significantly diminishes the spatial hole burning effect.

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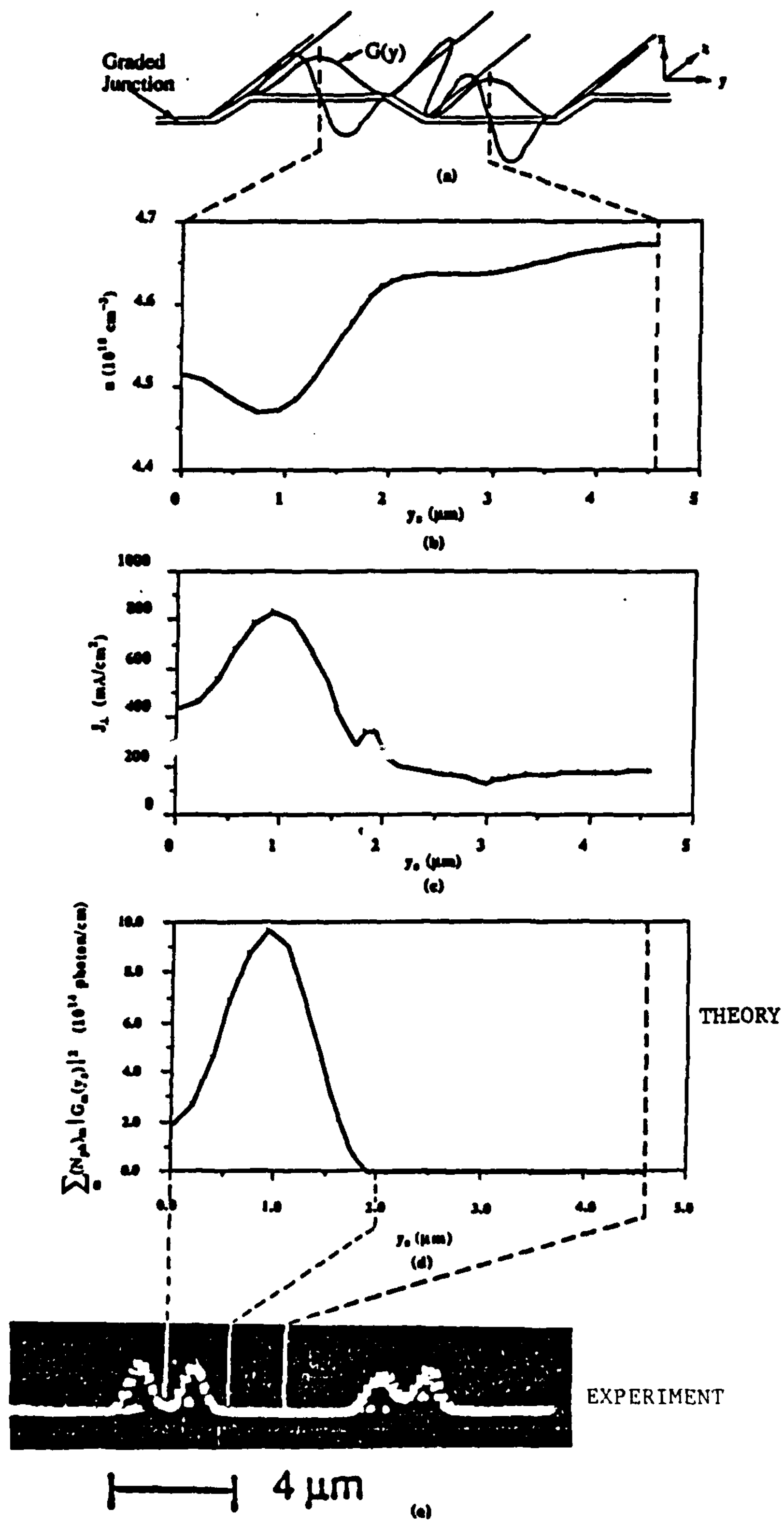


Fig. 1. Self-consistent solutions for the wafer I devices, (a) the structure and the optical modes, (b) the carrier concentration, (c) the injection current density, (d) the radiation optical mode, and (e) the experimental data.

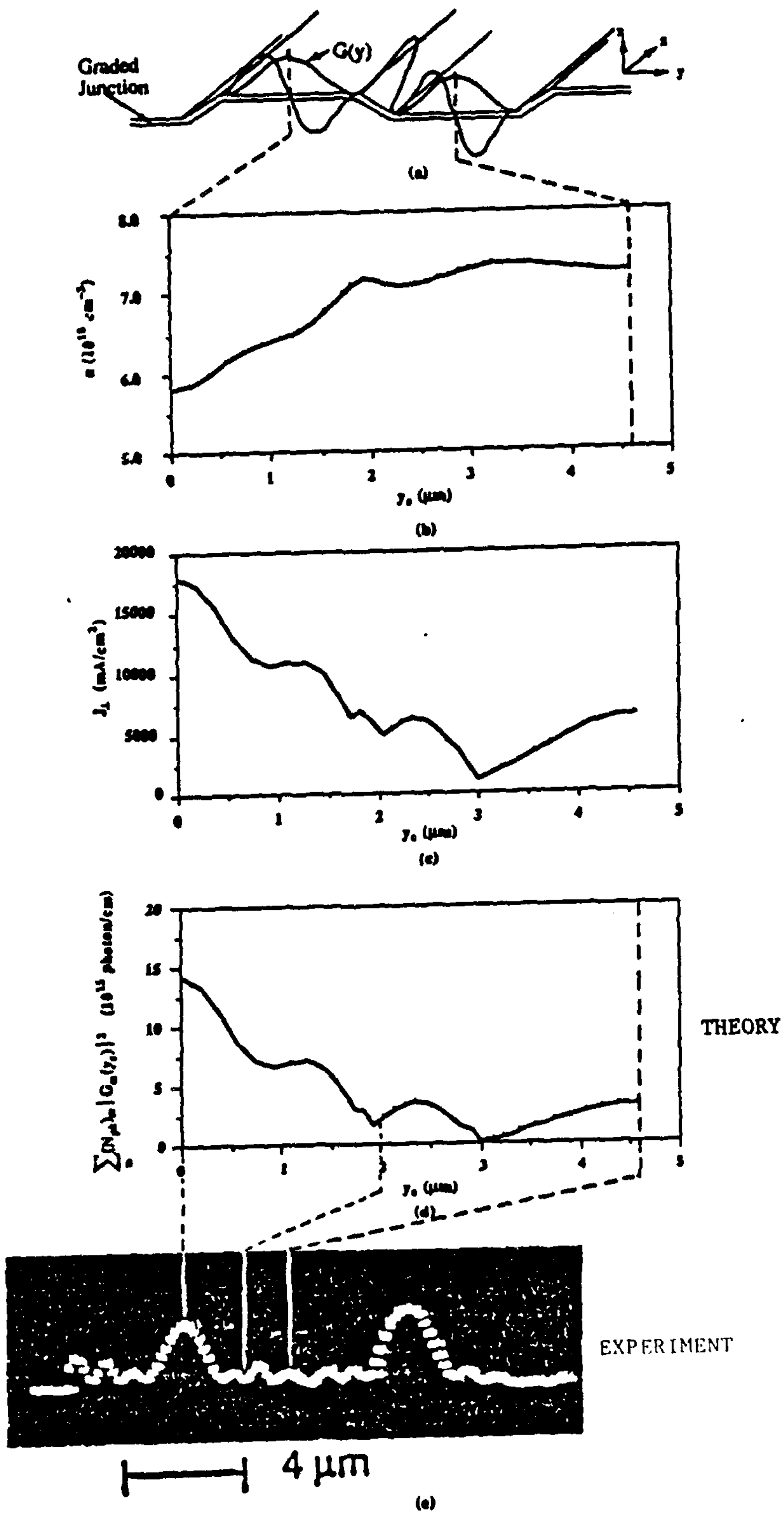


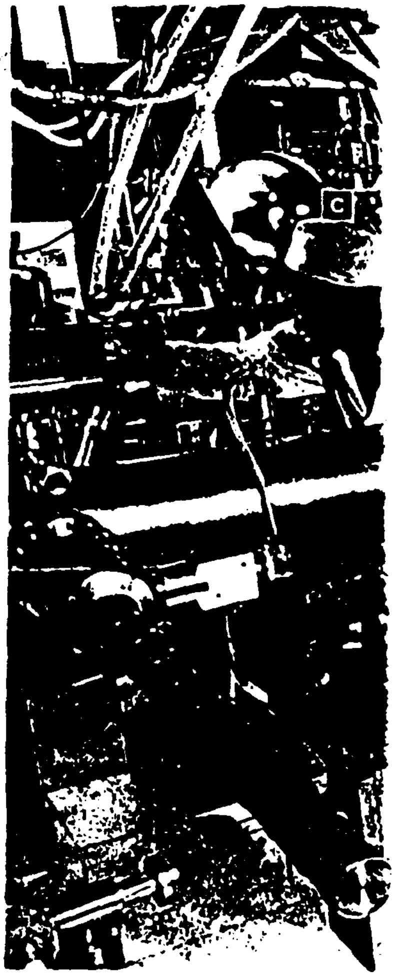
Fig. 2 Self-consistent solutions for the wafer II devices, (a) the structure and the optical modes, (b) the carrier concentration, (c) the injection current density, (d) the radiation optical mode, and (e) the experimental data.

APPENDIX

Grow and Analyze Complex Materials Like Never Before

Tying together seven molecular beam epitaxy chambers lets researchers create and analyze advanced materials.

By Tim Studt, Associate Editor, R&D Magazine



FROM THE OUTSIDE there's nothing special about the building. It's brick, the standard red variety, with your basic aluminum storm windows.

But inside the building, the second floor houses something very special in the world of atomic layer materials research.

That's where the Epicenter—the largest, most sophisticated molecular beam epitaxy research system in the world—resides.

In this one room, there is more stainless steel and more vacuum equipment than in most semiconductor manufacturing facilities. All of it is designed to make and analyze materials that will play a major role in the technologies developed during the next 20 years.

In the Epicenter, housed in the Coordinated Science Laboratory at Univ. of Illinois, Urbana, researchers have assembled seven molecular beam epitaxy (MBE) chambers and connected them with tubes. A transfer system inside the tubes allows researchers to freely move their samples, under ultrahigh vacuum, from one growth chamber to another.

This capability lets scientists use different MBE systems to grow and combine material layers that would be difficult to make in less sophisticated systems, if it could be done at all.

ESCA (electron spectroscopy for chemical analysis) and x-ray diffraction instruments also are integrated into this system. With these, the researchers can grow one atomic layer of a material, move it to the ESCA or x-ray system to examine its structure, move it to another growth chamber to deposit a different material, and then move it back to the ESCA.

The researchers can do all of this while maintaining the sample's environment at 10^{-11} torr, thereby minimizing contamination and undesired chemical effects.

So diverse are the material growth capabilities in the Epicenter that sponsorship was split among the university's Materials Research Lab, Coordinated Science Lab, and Center for Compound Semiconductor Microelectronics. While this arrangement can complicate accounting procedures, it brings together scientists who specialize in materials science, physics, and semiconductor design.

The principal researchers currently using the Epicenter are:

Hadis Morkoç, an associate professor of electrical and computer engineering who works in group III-V gas and solid source materials

Joseph Greene, a professor of metallurgy who works in ion and electron beam sources

Angus Rockett, an assistant professor of materials science and engineering who does work in group IV (silicon) materials

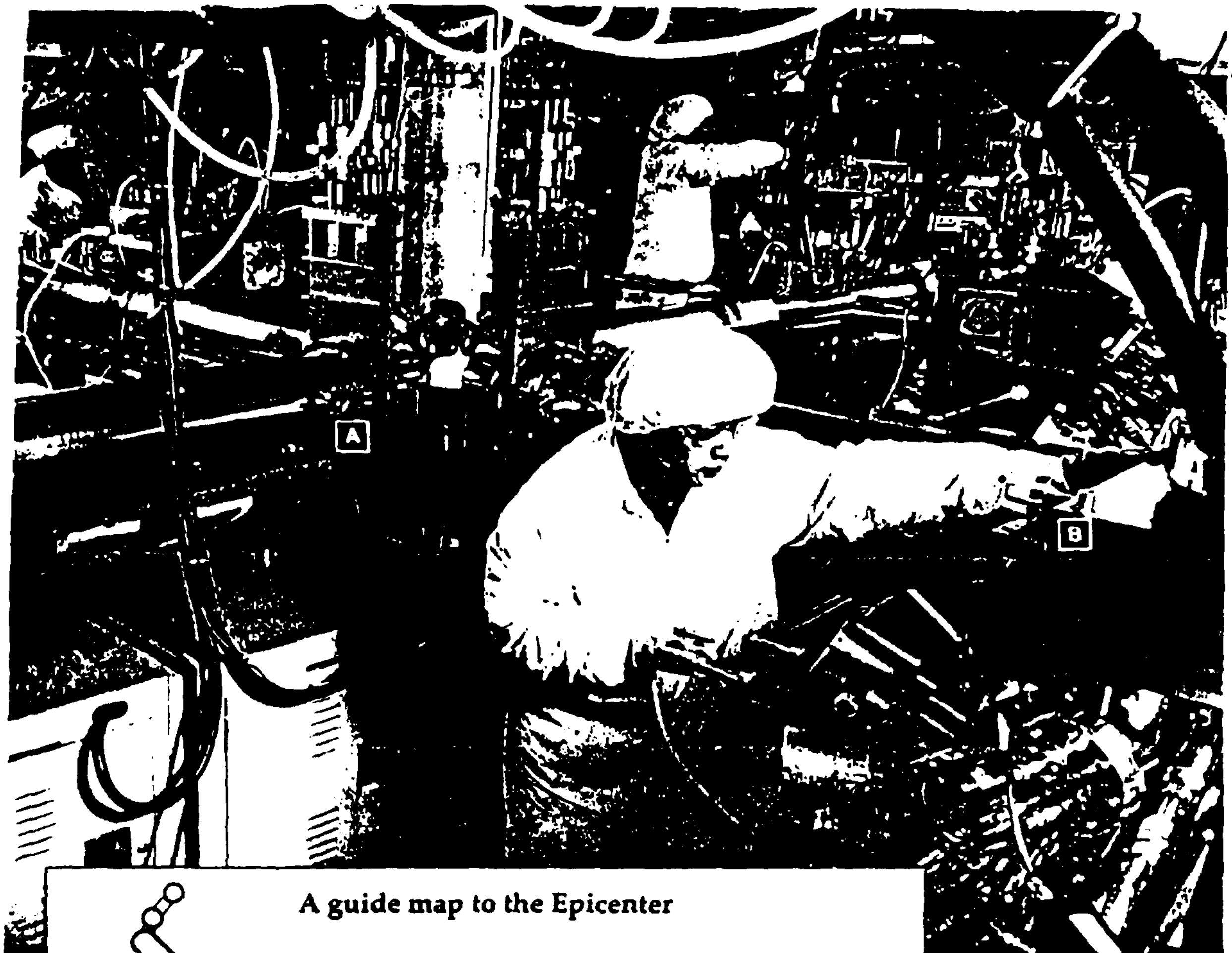
C. Peter Flynn, a professor of physics performing research in thin-film oxides and ceramics

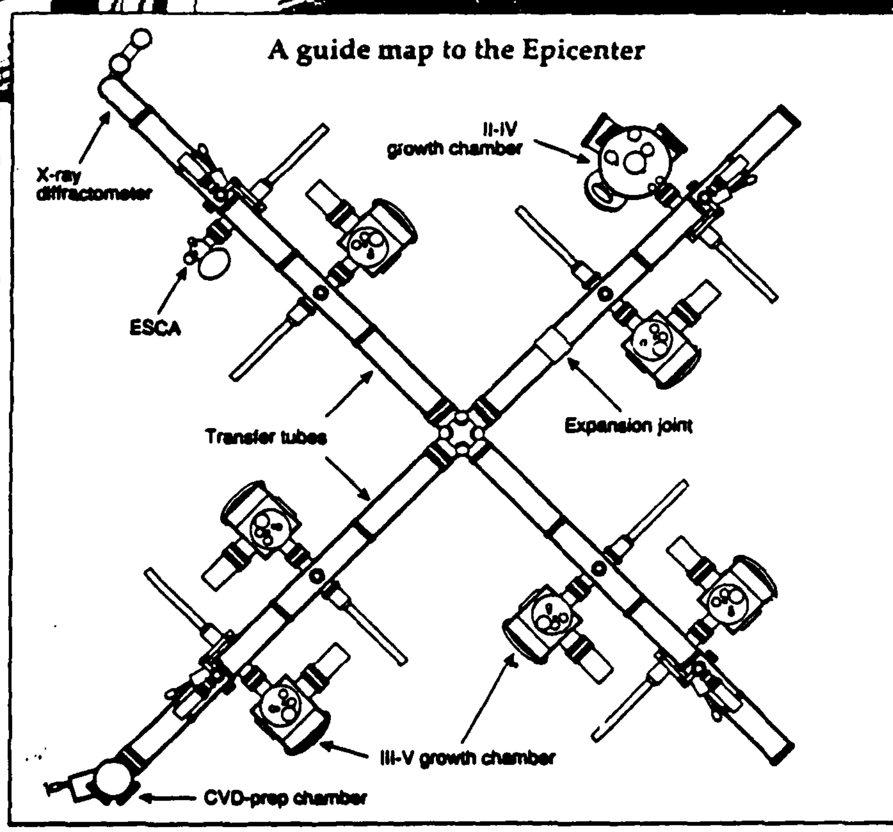
James Kolodzey, an assistant professor of electrical and computer engineering working on group III-V semiconductor devices

K. Y. Cheng, an *associate professor* of electrical and computer engineering also working on group III-V devices.

While these researchers have done work on smaller MBE systems, the Epicenter improves upon each of their previous research capabilities.

Additional analytical techniques used or being developed include ion,





Using a UHV transfer tube (A) system, researchers can move samples from one growth chamber (B) to another or to an ESCA instrument (C) in the Epicenter at Univ. of Illinois. The samples can be maintained at up to 10^{-11}-torr pressures throughout the transfer process.

At the Epicenter, scientists can grow material layers that would be difficult to make elsewhere.

Raman, and x-ray scattering, ellipsometry, and RHEED (reflection high-energy electron diffraction).

In an MBE chamber, a source material in a small container is heated, and the vaporized material is allowed to escape through a small hole, thus forming a purified beam of atoms. This beam of atoms combines with other beams to form larger molecules at a substrate surface, such as silicon or gallium arsenide. The molecules deposit in a crystalline-lattice structure that matches the substrate structure, thus forming an epitaxial layer.

Establishing a need

In many instances, one material in an MBE chamber cannot be used when another material is present. You cannot grow GaAs in the same chamber that you grow silicon, because arsenic is a dopant for silicon.

"Silicon technology is important, yet cleaning the silicon surface so that you can reconstruct materials on it is hard," says Epicenter researcher Peter Flynn.

Similarly, InGaAs, an important material in the development of monolithic optical and electrical device interfaces, "grows a 30-Å-thick oxide layer when exposed to air," says Epicenter researcher Jim Kolodzey.

Connecting several MBE chambers together with a UHV transfer tube provides the flexibility to deposit different layers of materials without contamination or material incompatibilities.

The Epicenter system is built around four sets of stainless steel transfer tubes connected to form an X.

The seven growth chambers and the ESCA instrument are placed at the ends of the tubes, with short access tubes between the chambers and the main transfer tubes. The ends of the main transfer tubes are designed for analytical or specialty functions.

An x-ray diffractometer is at the end of one main transfer tube, near the ESCA instrument. At the end of another tube is a chemical vapor deposition sample preparation chamber.

Everything you need to build an Epicenter

THE EPICENTER equipment at Univ. of Illinois cost about $7 million, part of which was subsidized by the supplier, Perkin-Elmer Corp., Eden Prairie, MN. To get a feel for the system's complexity, consider the following list of major components:

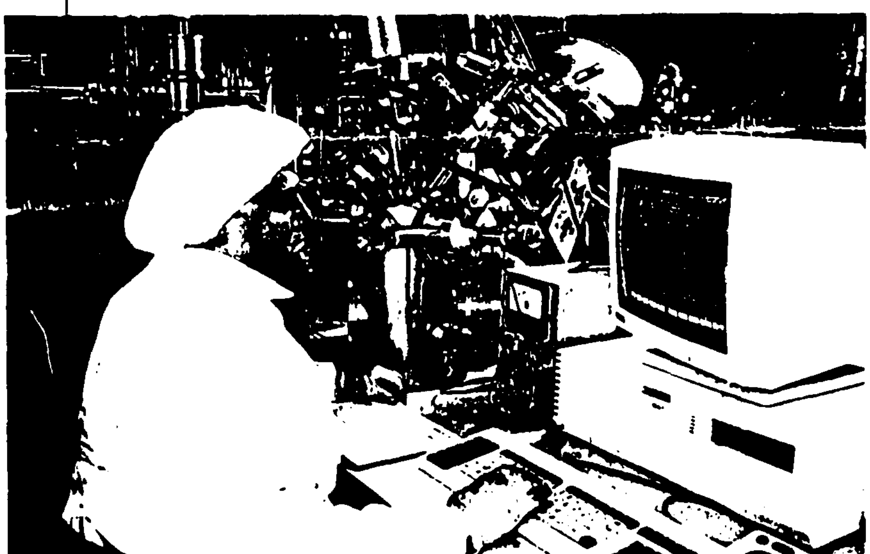
UHV chambers (>20 tons of steel)
7 MBE growth chambers
1 ESCA chamber
1 Triple-axis x-ray diffractometer
1 CVD-preparation chamber
4 Heated, UHV transfer tubes

Vacuum pumps
4 Mechanical pumps
3 Turbopumps
12 Cryopumps
24 Sorption pumps
12 Sputter ion pumps
11 Titanium sublimation pumps

Valves
42 Gate valves
18 Gold seal valves

Peripherals
7 Residual gas analyzers
78 Closed-loop controllers
4 Personal computers
6 E-beam gun systems
34 Fusion-cells
1,030 Vacuum seals
480 Feet of cryopump lines
18,500 Nuts and bolts

Add to this 10,000 gal of liquid nitrogen every month, 1,600-A electrical service needed to run the equipment, and molybdenum sample carriers—at $1,000 apiece!—used in the transfer tubes, and you start to understand the magnitude of this research system.



Researcher Boyd Bowdish uses an ESCA system to analyze epitaxial layers grown in a chamber 30 ft away. The samples were transferred to the ESCA under UHV.

Loading samples

Once exposed to the atmosphere, each of the seven main MBE chambers can take up to three days to pump down to 10^{-11} torr. To prevent exposure to the atmosphere, samples are loaded through smaller access ports on top of each transfer tube

The transfer mechanism consists of a sample carrier that rides on a trolley with ball-bearing wheels. The trolley moves through the tubes by a cable and pulley arrangement

At each chamber's access tube, a metal fork engages the sample carrier and moves it laterally into the growth chamber. Once in the growth chamber, another mechanism lifts and rotates the sample to a 25° orientation for final positioning.

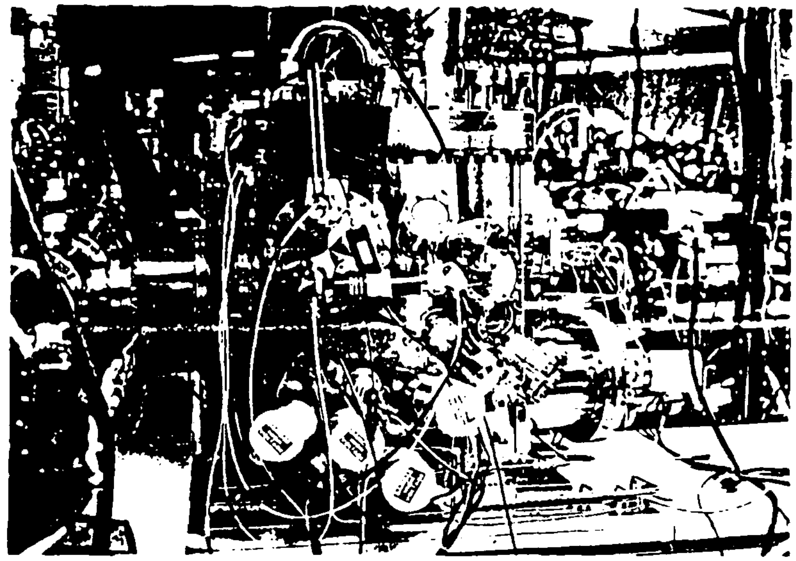
The transfer mechanism is manual and somewhat clumsy. Often, it takes up to 20 min. to go from one chamber to another. "You want to do it as few times as possible," says Flynn.

The simple mechanical arrangement minimizes the number of me-

Although the Epicenter is new, the researchers already have nine papers in print, with more to come.

The inside of a typical molecular beam epitaxial growth chamber (above) reveals eight independently operated shutters that cover the evaporation sources.

The Epicenter's silicon chamber (right) is larger than the other six chambers and provides more room for accessories, such as three e-beam guns.



chanical failures and contamination sources that an automatic system might involve.

The 9-in.-dia transfer tubes also serve as degassing and annealing chambers. A sample can be moved to a heated section of any transfer tube, where the material can be stabilized. Each of the four transfer tubes is pumped individually, so that as a sample degasses it will not put a load on the other vacuum systems.

Creating materials

Although the Epicenter only recently was completed, the principal researchers already have nine research papers in print concerning their Epicenter MBE research, with more to come.

Typical examples of this research include growth of GaAs on Si(100) surfaces, examination of the lattice orientations of GaAs on Ge, examination of Ge-GaAs and AlGaAs junctions, and growth of InGaAs devices with high mobilities.

A complex system like the Epicenter takes time to learn. "We're doing only 30% of what we want to do," says Morkoç.

The system does what it was designed to do, which is to make use of the different material deposition capabilities in each chamber. "About 50% of the MBE research being performed in the Epicenter currently involves transferring samples between chambers," says Morkoç.

Changes planned for the system include modifying the silicon chamber to allow germanium growth, adding an ion-beam patterning machine, and adding a scanning tunneling microscope.

Researchers beware

As with all technological systems, larger is not always better. Those who might want to consider building a similar system should consider the following warnings from Epicenter users.

First, check the reliability of the system. When you go to larger and more complex systems, total system reliability goes down. A system with only one chamber that is 80% efficient is inherently more reliable than a three-chamber system where each chamber is 90% efficient, since total reliability is 0.9^3 or 73%. "When you get too many machines, the system becomes complex and reliability becomes important," says Hadis Morkoç.

To compensate for the lower reliability of a large system, you must weigh the advantages of a simple, reliable MBE chamber design against a more sophisticated and potentially less reliable system design.

"Thermal expansion [of each tube] in the system also must be balanced," says Peter Flynn. The group-IV silicon growth chamber weighs more than the other MBE chambers. At first, when the full system was heated up, the thermal expansion of the tube with the silicon chamber was different than the thermal expansion of the other tubes. As a result, some mechanical systems jammed and an expansion bellows had to be retrofitted onto a transfer tube near the silicon growth chamber to solve the problem.

Finally, allow plenty of room for expansion. Even if you have enough space to build the world's largest system, always allow more space than you think you'll need for future expansion, says Jon Culton, manager of the Epicenter.

This applies to vertical and horizontal dimensions. The Epicenter's ceiling is so low that support wiring had to be hung from the ceiling instead of routed under a false floor.

Combining MBE chambers and systems is not a Univ. of Illinois monopoly. Similar systems, albeit smaller and not so complex, have recently been completed at Purdue Univ., Lafayette, IN, and at Univ. of Arizona, Tucson. The current trend in systematizing thin-film deposition processes likely will see more Epicenters in the future. R&D

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